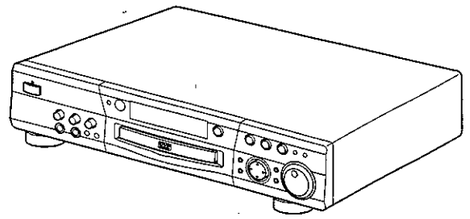
SERVICE GUIDE

DV-K2

DVD PLAYER	Marketed in July 1998 DVD No.B002

ADVICE

Please carefully read this guide before using the device. The Hitachi DVD Player has been designed to prevent fire, electrical shock, injury, or harmful radiation. It has been legally fabricated in accordance with the Electrical Appliances Act. Therefore, when using the device, please follow advice in this service guide to keep it safe to use.



1. In brief

DV-K2 is a device for DVD playback.
This device is to be used by connecting it to the video input terminal of a TV set.

2. Features

- ▶Disc navigation system facilitates program search.
- ▶Speedy operation by 2x speed drive.
- ▶Equipped with 2 mike input Karaoke

Contents

Specifications may be changed as improvements are made without advance notice. The marked price does not include consumption tax.

HITACHI

PRECAUTIONS FOR SAFETY (Please follow.)

Before undertaking repair work, please read through this [Precautions for safety].
The following points should be observed in order to prevent accidents from happening and to ensure the safety of the device.

● Degrees of danger or damage that can be caused by faulty operation are indicated by the following marks:

⚠ WARNING	Under this mark, there is "Possible death or serious injury".
⚠ CAUTION	Under this mark, there is "Possible injury or material damage".

● The following marks identify actions to be taken:

⚠	This mark indicates items to which 'You should pay attention'.	❗	This mark indicates items 'You have to accomplish'.
⚠	This mark indicates: 'You should be cautious of electric shock'.	⊘	This mark indicates 'Forbidden items"

⚠ WARNING

■You should pay attention.

⚠ Where a special attention is required, it is indicated by a label or stamp. For example, on the cabinet, chassis, or parts.
Please respect the indicated items and the 'Precautions for use' of the manual.

■You should be cautious against electric shock.

⚠ Please be careful during operations because there are high voltage and recharging parts inside. An electric shock or death may happen by touching them.
When disassembling, assembling, or replacing a part, the power plug has to be pulled off.
Touching by error a powered part may cause an electric shock, death, or injury.

■Please use designated parts.

❗ Parts are characterized by uninflammability and voltage resistance. Therefore, parts having these same characteristics must be used in replacement.
Especially for parts important in insuring safety, identified by ⚠ in the wiring diagram or parts list, a part with the identical part number shall be used.
If a part with a different part number is used, an electric shock or a fire may occur.

■The original part installation and wiring route shall be restored.

❗ For safety, some parts are insulated by a tube or a tape, or installed without contact with substrate. The internal wiring is kept a distance from hot or high voltage parts by clamps or routing. Please restore them as initially done to prevent electric shock or fire from happening.

■Please check safety after servicing.

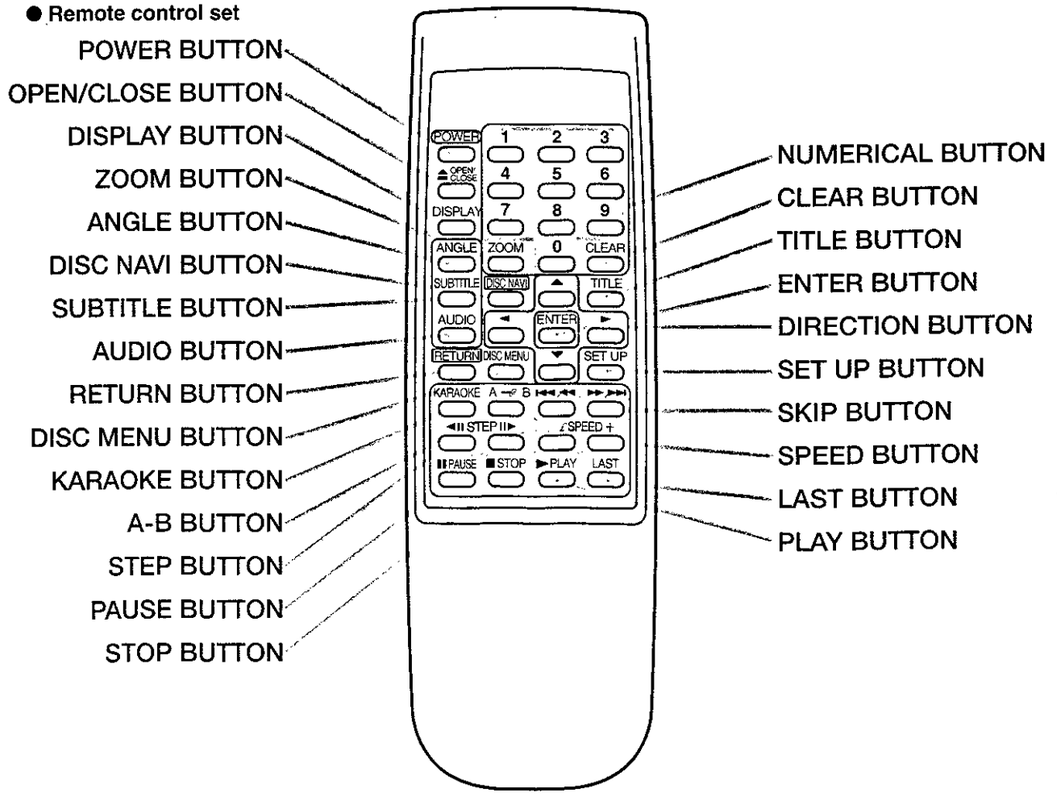
❗ Please check if dismounted screws, parts, and wires are reinstalled as before and if the area surrounding the repair is damaged.
Please also measure insulation resistance with a ohmmeter and to confirm that it is more than 1M Ω.
There is risk of electric shock or fire if the insulation resistance is less than 1M Ω.

3. Specification

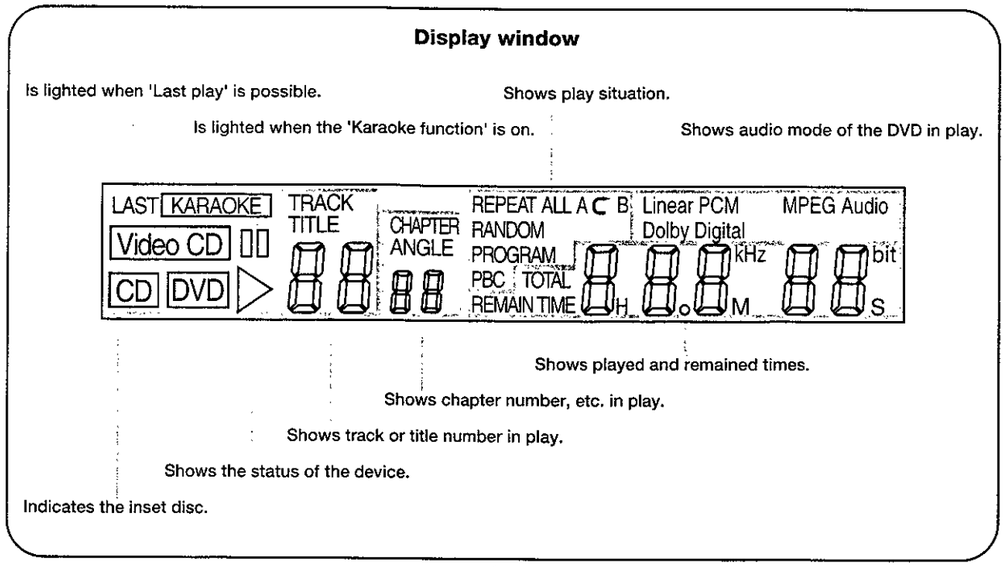
Common			
Model Laser type Electric energy Power	DV-K2 Semiconductor laser Wave length:650nm (DVD), 780nm(CD,VCD) AC100V,50/60Hz both 22W	Mass Overall size Allowable operating temperature Allowable operating humidity	4.1 kg 43.4(W)X31.5(D)X9.8(H)cm +5℃~+35℃ 15%~75%(without condensation)
S image output terminal [1 system] (S2 output)			
Y output level C output level	1Vp-p (75 Ω) 286mVp-p (75 Ω)	Output terminal	S terminal
Image Output terminal [1 system]			
Output level	1Vp-p (75Ω under load, synchronous negative)	Output terminal	Pin jack
Audio output terminal [2 systems]			
Digital audio output level Channels <Digital audio characteristics> Frequency characteristics	200mVrms(1KHz,-20dB) 2 channels CD:4Hz~20KHz(EIAJ) DVD:4Hz~22KHz(48K sampling)	Frequency characteristics (continued) SN ratio Dynamic range Total high frequency distortion rate Wow flutter	DVD:4Hz~44KHz(96K sampling) 110dB 100dB 0.003% Measuring limits: less than (±0.001%W.PEAK) (EIAJ)
Other terminals			
Optical digital output: (Dolby Digital <AC-3>/LPCM,LPCM, may be switched to OFF) optical connector			
Accessories			
Remote control (DV-RM2) Single3 type battery (R6P)	1 2	AV cord Power cord	1 1

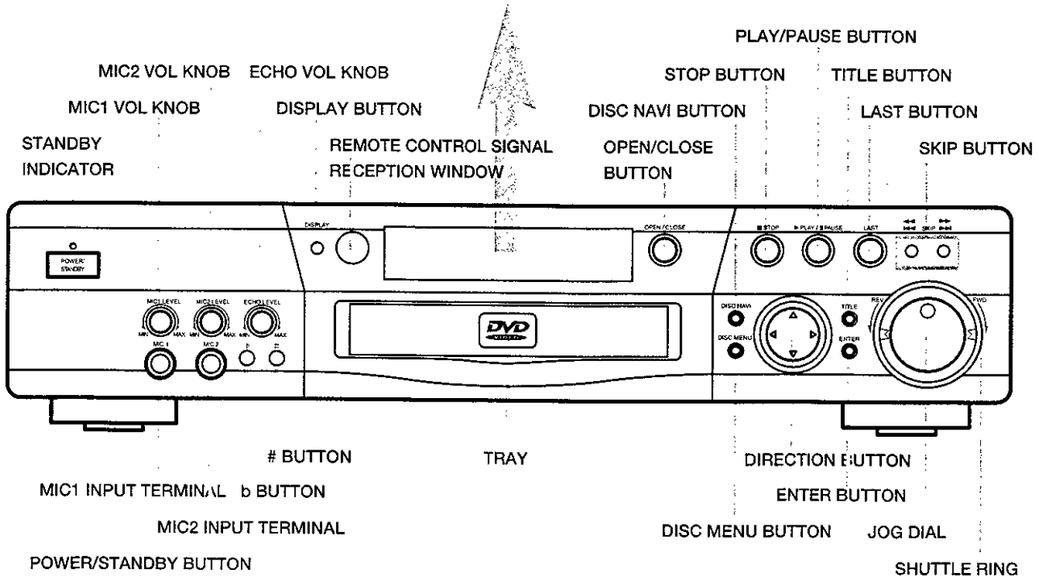
4. Name of parts

● Remote control set

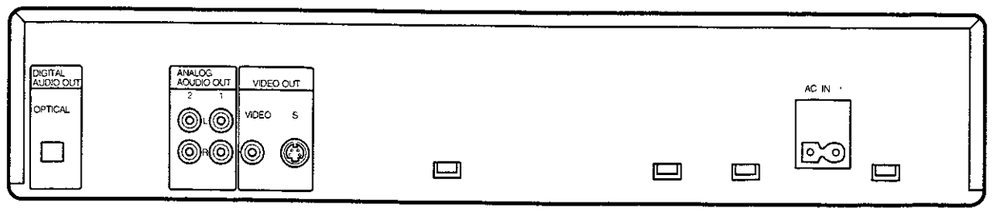


● Front face





● REAR SIDE



AUDIO OUTPUT TERMINALS
S IMAGE OUTPUT TERMINAL
OPTICAL DIGITAL AUDIO OUTPUT TERMINAL
IMAGE OUTPUT TERMINAL
POWER CORD CONNECTING TERMINAL

5. Description of adopted new technology

5-1 Digital signal circuit

(1) Data flow

Fig. 5-1 shows the block diagram of digital signal circuit.

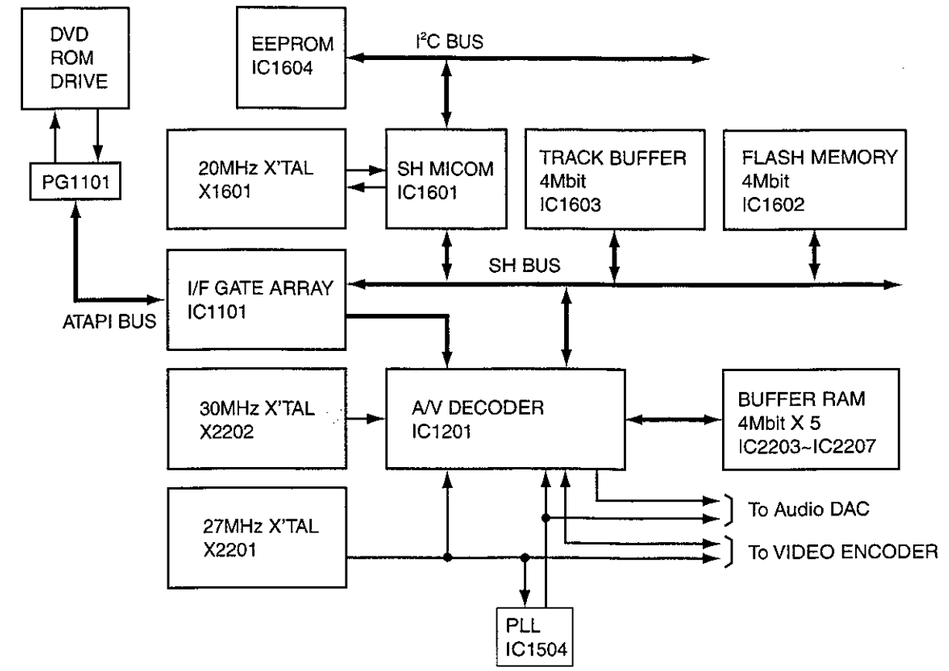


Fig. 5-1 Block diagram of digital signal circuit

DISC data read by DVD ROM DRIVE are stored in TRACK BUFFER (IC1603) by SH MICOM (IC1601) and through I/F GATE ARRAY (IC1101). Then the stored data will be read out from TRACK BUFFER in response to demand by A/V DECODER (IC1201) and input in A/V DECODER through I/F GATE ARRAY. Finally, A/V DECODER will demodulate/decode the data according to their contents and output Audio data to Audio DAC(IC1502), and video data to Video ENCODER(IC2202)

(2) Reference clock of each IC

IC	Reference Clock
IC1101 I/F GATE ARRAY	20MHz clock generated by SH MICOM
IC1601 SH MICOM	System clock of X1601 20MHz X'TAL, SH
IC1602 FLASH MEMORY	Nil (Control signal is generated by SH MICOM)
IC1603 TRACK BUFFER	Nil (Control signal is generated by SH MICOM)
IC1604 EEPROM	Nil (Control signal is generated by SH MICOM)
IC1201A/V DECODER	• System clock is input from X2202 30MHz X' TAL. • Video interface clock is input from X2201 27MHz X' TAL. • Audio interface clock is input from IC1504 PLL 16.934 (18.432, 36.864) MHz.
IC1504PLL	16.934 (18.432, 36.864) MHz is generated by X2201, 27MHz X' TAL input.

(3) Functions of each IC

	IC	Functions	Operating voltage
①	IC1101 I/F GATE ARRAY	Execute data transfer timings from ATAPI to TRACK BUFFER, and from TRACK BUFFER to A/V DECODER.	5V
②	IC1601 SH MICOM	Execute data transfer, presetting and control of each IC.	5V
③	IC1602 FLASH MEMORY	Store memory for SH MICOM software	5V
④	IC1603 TRACK BUFFER	Buffer memory for data transfer	5V
⑤	IC1604 EEPROM	Storage memory for LAST KEY operation data	5V
⑥	IC1201 A/V DECODER	Execute decompression (decoding) of data compressed by MPEG	3.3V
⑦	IC2203~IC2207 BUFFER RAM	Memory used for decompression (decoding) of data compressed by MPEG and controlled by A/V DECODER	5V
⑧	IC1504 PLL	Generate 16.934 (18.432, 36.864) MHz of audio interface signals from 27MHz clock.	5V

The following is the description of the functions of each IC:

① I/F GATE ARRAY (IC1101)

It executes signal timing changes between SH MICOM (IC1601) AND DVD ROM DRIVE I/F (PG1101),A/V DECODER (IC1201). It operates on 20MHz clock output from SH MICOM.

② SH MICOM (IC1601)

It transfers data and executes presetting and control of each IC.

Data transfer from DVD ROM DRIVE I/F is done by setting a register of I/F GATE ARRAY and by intermediary of I/F GATE ARRAY.

In addition, it controls Audio DAC ((IC1502), VIDEO ENCODER (IC2202), AND EEPROM (IC1604), manages TRACK BUFFER (IC1603) AND FLASH MEMORY (IC1602), and communicates with FL MICOM (IC1701).

With 20MHzXTAL(X1601) attached it pulses and is used as a SYSTEM CLOCK.

③ FLASH MEMORY (IC1602)

A 4Mbit FLASH ROM is used. It stores SH MICOM program and its access is controlled by SH MICOM.

④ TRACK BUFFER (IC1603)

A 4Mbit DRAM is used. It stores data read out from DISC. Its control is done by SH MICOM, and its data is read-written via IF/ GATE ARRAY. In addition a part of this BUFFER is used as the WORK AREA of SH MICOM.

⑤ EEPROM (IC1604)

It is a 16Kbit EEFROM and stores DISC information by LAST KEY, etc. SH MICOM controls it.

⑥ A/V DECODER (IC1201)

Data input from TRACK BUFFER via I/F GATE ARRAY is separated into Audio data and Video data. MPEG compressed data are decompressed (decoded) and output as DIGITAL Video and DIGITAL audio (AC-3). SH MICOM controls it via I/F GATE ARRAY. SYSTEM CLOCK, CLOCK of VIDEO INTERFACE signals, and CLOCK of AUDIO INTERFACE signals operate by inputting 30MHz, 27MHz, and 16.934(18.432, 36.864)MHz, respectively.

⑦ BUFFER RAM (IC2203~IC2207)

Five 4 Mbit DRAM are used. A/V DECODER controls it and it is used to decompress Audio and Video data compressed by MPEG.

⑧ PLL (IC1504)

PLL generates 16.934(18.432, 36.864)MHz of AUDIO INTERFACE signals clock by inputting 27MHz from VIDEO INTERFACE signals clock. It supplies A/V DECODER and Audio DAC. (See 5-8 clock circuit.)

5-2 Video circuit (DEC substrate)

8bit YC_RC_B DIGITAL VIDEO STREAM (P) output from A/V DECODER is input in VIDEO ENCODER B1865A (IC2202). VIDEO ENCODER is preset in IC in MASTER MODE that generates reference signals and receives 27MHz from SYSTEM CLOCK and outputs H,V synchronous signals to A/V DECODER.

By presetting of internal register, VIDEO DECODER generates:

① NTSC (North America, Japan, Taiwan)

② PAL (Europe, Asia)

standard analog video signals.

Filter circuit eliminates high frequency components of analog video signals output from VIDEO DECODER. Afterwards in S2 processor circuit DC voltage is superposed on C signals then output 2 types of video signals: COMPOSITE VIDEO SIGNALS and Y/C(S2) VIDEO SIGNALS to RJK substrate via 6P connector (PG2201).

The following is a description of VIDEO CIRCUIT along signal flow:

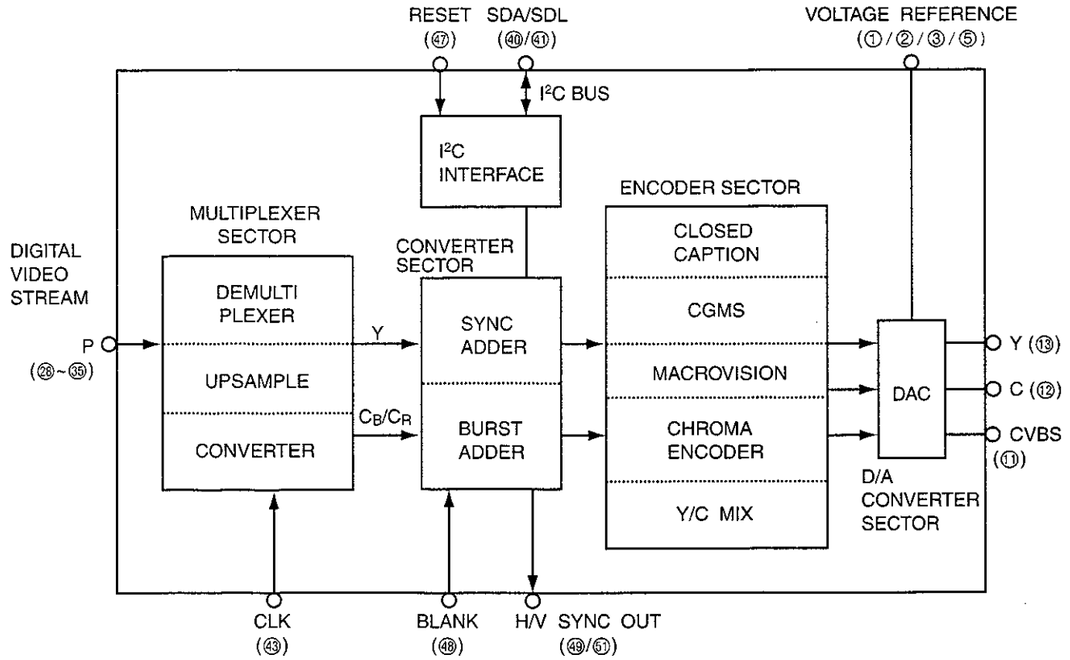


Fig. 5-2-1 Block diagram of VIDEO ENCODER B1865A (IC2202) interior

5-2-1 VIDEO ENCODER B1865A (IC2202)

(1) MULTIPLEXER SECTOR

It transforms input DIGITAL VIDEO STREAM (Input at ㉘~㉟ pins) in 8bit parallel data then separates them in Y DATA and C_B/C_R DATA and changes simultaneously the rate (6.75MB/S→13.5MB/S).

(2) CONVERTER SECTOR

It generates various internal timing signals with the synchronous signal as standard by adding synchronous signals generated in IC to Y DATA, according to the conditions set in the internal register or by adding BURST signals to C_B/C_R DATA. At the same time it outputs these synchronous signals to A/V DECODER (Output at ㊾,㊿ pins). BLANK signal (Input of L level at ㊽ pin) is input from SH MICOM when power is turned ON or OFF to prevent screen flickering. In addition, when power is turned ON, RESET signal (Input of L level at ㊼ pin) is input to reset the register in IC.

Moreover, writing in the internal register (presetting) is done via I²C BUS (㊵,㊶ pins).

(3) ENCODER SECTOR

The following ①~③ data are inserted in VIDEO DATA according to preset conditions in the internal register:

① Closed caption

NTSC Mode: 21 lines and 284 lines/ PAL Mode: 22 lines and 335 ines.

② CGMS (Copy Guard Management System)

20 lines and 280 lines of NTSC.

③ Macrovision Copy Prevention System

Finally it generates DIGITAL INTENSITY DATA, DIGITAL CHROMA DATA, and DIGITAL COMPOSITE DATA.

(4) D/A CONVERTER (DAC)SECTOR

Constituted of 10bit DAC, it transforms DIGITAL VIDEO DATA in ANALOG VIDEO DATA for output. Under control of output voltage by DAC pins (①, ②, ③, ⑤pins), it output 3 kinds of ANALOG VIDEO SIGNALS:

① ANALOG COMPOSITE VIDEO SIGNALS (CVBS/⑪ pin), output voltage 1.0Vpp.

② ANALOG INTENSITY SIGNALS (Y/⑬ pin)., output voltage1.0Vpp.

③ ANALOG CHROMA SIGNALS (C/⑫ pin), BURST part output voltage 286mVpp.

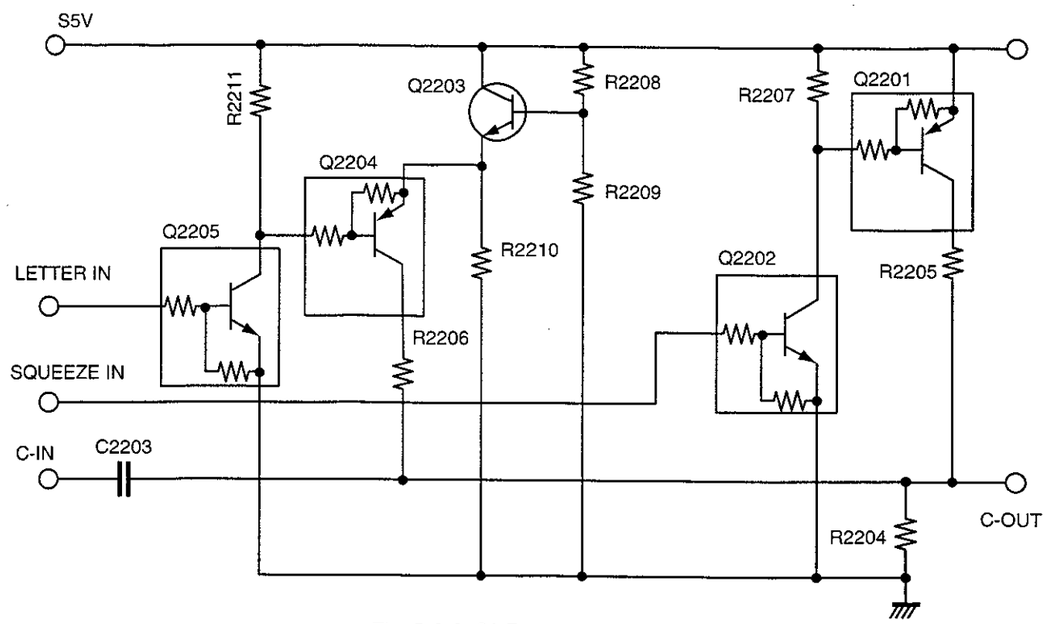


Fig. 5-2-2 S2 Processing Circuit

5-2-2 S2 Processing Circuit

S2 is a standard used in wide television sets possessing screen size switching function in NTSC mode. By inputting VIDEO signals formed by superposing DC voltage on C signal at S input terminal, it switches automatically to TV display size. The DC voltage superposed on C signal varies according to the ASPECT RATIO of VIDEO SIGNALS.

(1) Case of SQUEEZE SIGNAL (*1)

H-level voltage is input in SQUEEZE INPUT; Q2202 and Q2201 are powered and +4V DC voltage is superposed on C signal output line.

(2) Case of LETTER BOX SIGNAL (*2)

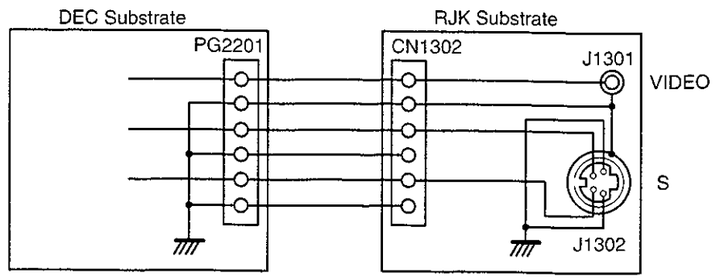
H-level voltage is input in LETTER INPUT; Q2205, Q2204, and Q2203 are powered and +1.8V DC voltage is superposed on C signal output line.

*1: It is a laterally shrunk image information with 525 lines and an aspect ratio of 16:9 carried by the standard TV signal format of 525 lines and an aspect ratio of 4:3. When viewing on a 4:3 TV set, the image appears vertically oblong.

*2: It is a wide screen signal in the standard TV signal format of 525 lines and an aspect ratio of 4:3 with coexistence of upper and lower blank areas of 525 lines and an aspect ratio of 4:3 screen and the principal image area of 4:3 aspect ratio (line 53~232/316~495). When viewing on a 4:3 TV set, one sees black areas at the top and bottom of the screen.

5-3 VIDEO OUTPUT CIRCUIT (RJK substrate)

ANALOG COMPOSITE VIDEO SIGNALS (CVBS), ANALOG INTENSITY SIGNALS (Y), and ANALOG CHROMA SIGNALS (C) are sent from DEC substrate to RJK substrate by passing through 6P connector (PG2201~CN1302). From RJK substrate, CVBS signals are output from output terminal J1301 and Y/C signals are output from output terminal J1302.



5-4 AUDIO CIRCUIT

AUDIO CIRCUIT is shown in Fig. 5-4-1.

AUDIO CIRCUIT is composed of D/A CONVERTER SECTOR (DEC substrate) that transforms digital audio signals output from A/V DECODER (IC1201), ANALOG PROCESSING SECTOR (RJK substrate) that consists of an operational amplifier, and MUTE CIRCUIT (DEC substrate, RJK substrate) for stopping audio output when required.

(1) D/A CONVERTER SECTOR (DEC substrate)

D/A CONVERTER SECTOR is composed of IC1502 that receives and transforms digital audio signals from A/V DECODER in analog signals and IC1504 that generates clock signals corresponding to the sampling frequency of digital audio signals from 27MHz of master clock signals.

IC1502 is a converter corresponding to L and R signals of sampling frequencies 44.1/48/96kHz and data lengths16/20/24bit, and digital audio signals from A/V DECODER is input at ② pin.

To these digital audio signals are inserted L and R signals in time sharing mode. When they are input in ① pin, they are separated in L and R signals by R clock and after transformation analog L signals are output at ⑯ pin and R signals at ⑬ pin. Moreover, when there are no input signals at ② pin, a signal called ZERO MUTE is output to ㉑ pin to mute useless noises (See paragraph on MUTE CIRCUIT.)

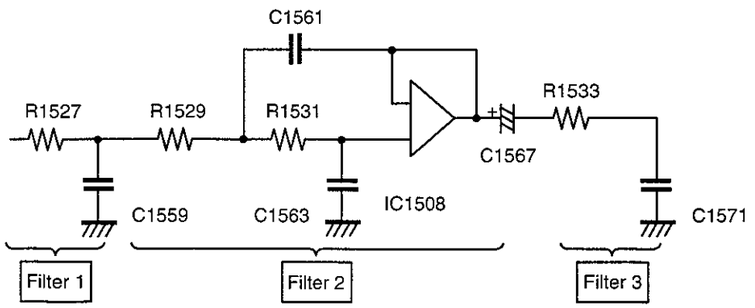
Every functions of IC1502 is preset by MICOM and controlling signals from SH MICOM are input at ㉖㉗㉘ pins. As for presetting items, there are data length, sampling frequency, signal polarity, and de-emphasis.

On the other hand, 27MHz master clock is input at ① pin of IC1504, then passes through the internal PLL circuit and is output from ② pin as a clock signal provided to IC1502.

(2) ANALOG PROCESSING SECTOR (RJK substrate)

ANALOG PROCESSING SECTOR is composed of operational amplifier IC1508 that is a filter and operational amplifier IC1510 that mixes and amplifies audio signals and Karaoke signals.

Filter portion is composed of RC low bass filter and IC1508 formed active low bass filter and there are 3 sections. The diagram below shows its filter portion circuit (for L signals only).



This 3-section filter constitutes a low bass filter of overall cutoff frequency of 44kHz. Audio signals after low bass filter is amplified by IC1510 by about 6dB and output to AUDIO OUT1 AND AUDIO OUT2.

Here, among audio signals, L signals are input at ③ pin of IC1508 and output from ① pin, then input to ② pin of IC1510 then output from ① pin.

R signals are input at ⑤ pin of IC1508 and output from ⑦ pin, then input to ⑥ pin of IC1510 then output from ⑦ pin.

(3) MUTE CIRCUIT (DEC substrate, RJK substrate)

The principal role of MUTE CIRCUIT is the erasing of useless noises occurring when power is turned on.

Mute signal for noise erasing is generated by SH MICOM, reverse-amplified by Q1505 and Q1506. Then by putting Q1510, Q1511, Q1310, and Q1311 'ON', it mutes audio signals.

In addition, if IC1502 detects no-signal, it generate a mute signal called ZERO MUTE. This latter is reverse-amplified by Q1507 and mutes useless audio signals by putting Q1310 and Q1311 'ON'.

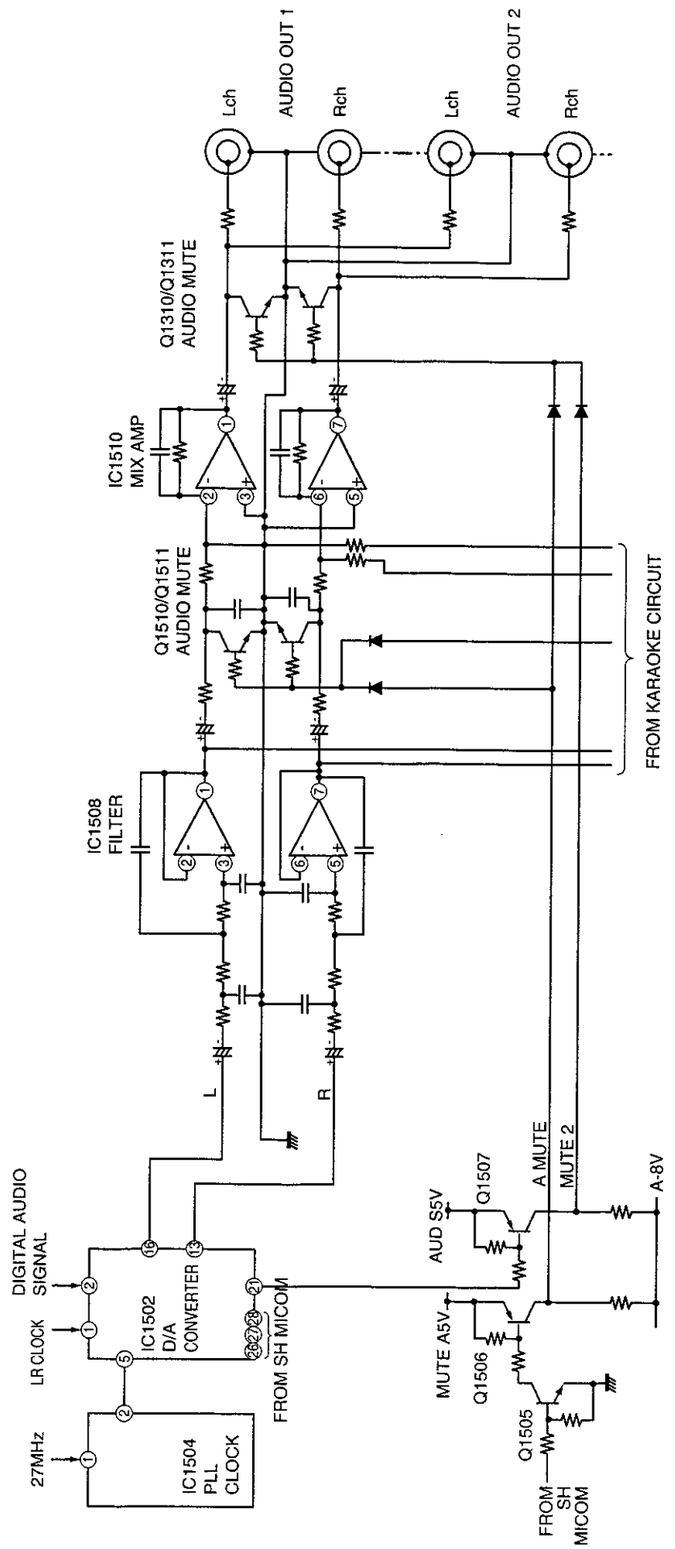


Fig. 5-4-1 Audio circuit

5-5 KARAOKE CIRCUIT (The following descriptions concern Lch signal/Rch signal) When mike is connected to the mike input terminal. "KARAOKE" will be lighted on FL tube and mode will be changed to Karaoke mode. Therefore, karaoke functions of keycon and vocal cancel may be used. When mike is disconnected, karaoke mode is 'OFF'.

(1) MAIN CIRCUIT

L/Rch signals output by audio circuit low bass filter, IC1508 ①, ⑦ pins pass through BUFFER (IC1509, input at ③, ⑤ pins, output at ①, ⑦ pins) and are input to IC1417 at ㉗, ㉘. Then they are processed and sorted, by command by SH MICOM (IC1417, input at ㉝, ㉞ pins), in Lch MONO*1, Rch MONO*2, VOCAL CANCEL*3, L/Rch output as it is, and then output from ㉘, ㉙ pins.

Afterwards, L/Rch signals pass through HPF (IC1418, input at ⑳ pin, output at ⑲/ IC1419, input at ② pin, output at ① pin), mixed with MIKE ECHO signal and KEYCON signal (IC1418, input at ⑯ pin, output at ⑮ pin/IC1419, input at ⑥ pin, output at ⑦ pin), pass switch IC that is used as keycon alternate cicuit (IC1421, input at ④, ⑧ pins, output at ③, ⑨ pins), and finally flow back to the audio circuit (IC1510, input at ②, ⑥ pins).

*1 Lch MONO: Lch signals output at L/Rch.

*2 Rch MONO: Rch signals output at L/Rch.

*3 VOCAL CANCEL: Vocal portion situated in the center of vocal source is attenuated.

(2) KEYCON CIRCUIT

L/Rch signals output from IC1417, ㉙, ㉘ pins, is mixed with Lch and input to IC1418, ㉗ pin. After flowing through LPF, they enter KEYCON CIRCUIT to receive KEYCON process according to command from SH MICOM (IC1418, input at ⑦, ⑧, ⑨ pins) and are output at ⑳ pin.

After that , they flow again through LPF (IC1418, input at ⑱ pin, output at ⑰ pin) and are mixed with main L/Rch signals input at IC1418 ⑯ pin/IC1419 ⑥ pin.

As described above, signals flowing through LPF are mixed with L/Rch, so that when KEYCON is operating (Otherwise there is alternativecircuit.), they become pseudo stereo. LPF makes KEYCON process signals below ~3.3kHz.

(3) KEYCON ALTERNATIVE CIRCUIT

To prevent signals from becoming always pseudo stereo due to KEYCON CIRCUIT, they are arranged to flow in an alternative circuit when the key is natural (When KEYCON is not operating.).

Signals to be output to audio circuit are switched by inputting signals before and after KEYCON process to SWITCH IC, IC1421. Signals before KEYCON process are output at IC1417 ㉙, ㉘ pins and input at ①, ⑪ pins. Signals resulting from the mix up of KEYCON signals and MIKE ECHO signals are output at IC1418 ⑬ pin/IC1419 ⑦ pin and input to IC1421 ④, ⑧ pins.

Control signal, KEYFO (Hi, when key is natural; Lo, otherwise) from SH MICOM is input to Q1423, then flows through Q1424 to reach IC1421 ⑬, ⑫ pins. Finally signals flow through Q1425 from Q1424 and reversed is input to IC1421 at ⑤, ⑥ pins. With this control signal, input at IC1421 ①, ⑪ pins is output at ②, ⑩ pins; otherwise, input at IC11421④, ⑧ pins is output at ③, ⑨ pins. Signals output from IC1421 flow back to AUDIO CIRCUIT and are input at IC1510 ②, ⑥ pins.

When key is natural, signals flow outside MIKE ECHO signal mix circuit, therefore with KEYFO (input at IC1417 ㉛ pin), MIKE ECHO signals are mixed with L/Rch signals in IC1417 and output at IC1417 ㉘, ㉘ pins.

(4) MIKE-ECHO CIRCUIT

Signals output from MIC1 are input to IC1417 ① pin, then after passing through MIKE amplifier, output to MIKE VOLUME RV1762 from ④ pin, then input again to IC1417 at ⑤ pin. Similarly, signals output from MIC2 are input to IC1417 ⑥ pin, then after passing through MIKE amplifier, output from ⑨ pin to MIKE VOLUME, then input again to IC1417 at ⑩ pin.

MIC1 and MIC2 are mixed inside IC1417 then output from ⑪ and input at ⑫ pin. After ECHO process they are output from ㉔ pin, pass through ECHO VOLUME RV1764, and input again to IC1417 ㉖ pin. In IC1417, signals input at ㉕ pin are mixed with the mixed signals, as said above by MIC1 AND MIC2, then output from ㉚ pin. Afterwards, they are input at IV1418 ⑱ pin/IC1419 ⑥ pin, and mixed with L/Rch signals.

(5) KARAOKE ALTERNATIVE CIRCUIT

In order to prevent deterioration of common audio sound, it is designed that Karaoke signals pass KARAOKE CIRCUIT only in Karaoke mode (i.e., when mike is connected.)

MIC SW (output from MIC2 jack J1763 ⑤ pin) used as control signal is [Hi] when either of MIC1 or MIC2 is, or both are connected. Otherwise it is [Lo].

After passing through Q1417, MIC SW is connected to Q1419/Q1418. After passing through Q1417, MIC SW passes Q1420 and is connected to Q1511/Q1510. Q1511/Q1510 are connected to output IC1508 ①, ⑦ pins of audio circuit filter. Moreover, after passing through Q1417, MIC SW is connected to Q1422/Q1421. Q1422/Q1421 are connected to output IC11421 ③. ⑨ pins of Karaoke circuit.

In Karaoke mode, signals are output by setting Q1419/Q1418 t 'OFF'.

When Karaoke mode is 'OFF', signals input in Karaoke circuit are muted by setting Q1419/Q1418 'ON'. In addition, output signals of Karaoke circuit are muted by putting Q1511/Q1510 'OFF' and muting audio signals.

(6) VOICE SW

It detects audio input in mike, and is used in AUTO VOCAL CANCEL or to playback mike input without music. Signals having passed are mixed after output from IC1417 ④ pin (MIC1) and ⑨ pin (MIC2). Then, they are input to IC1420 ③ pin, output from ⑦ pin in DC, and finally input to Q1426 base. When sound enters mike, Q1426 is put 'ON' and collector becomes [Lo]. If no sound enters mike, Q1426 is put 'OFF' and collector become [Hi]. This collector output is named VOICE SW. VOICE SW is input to SH MICOM and used for AUTO VOCAL CANCEL control. In addition, it passes through Q1504 and Q1507 of DEC substrate, sets Q1310/Q1311 to 'ON' or 'OFF', and controls muting of audio output. In general, when there is no audio output, there is no noise output, muting is effective on audio output. When there is mike input, it puts Q1310/Q1311 'OFF', lets mike input output without being muted.

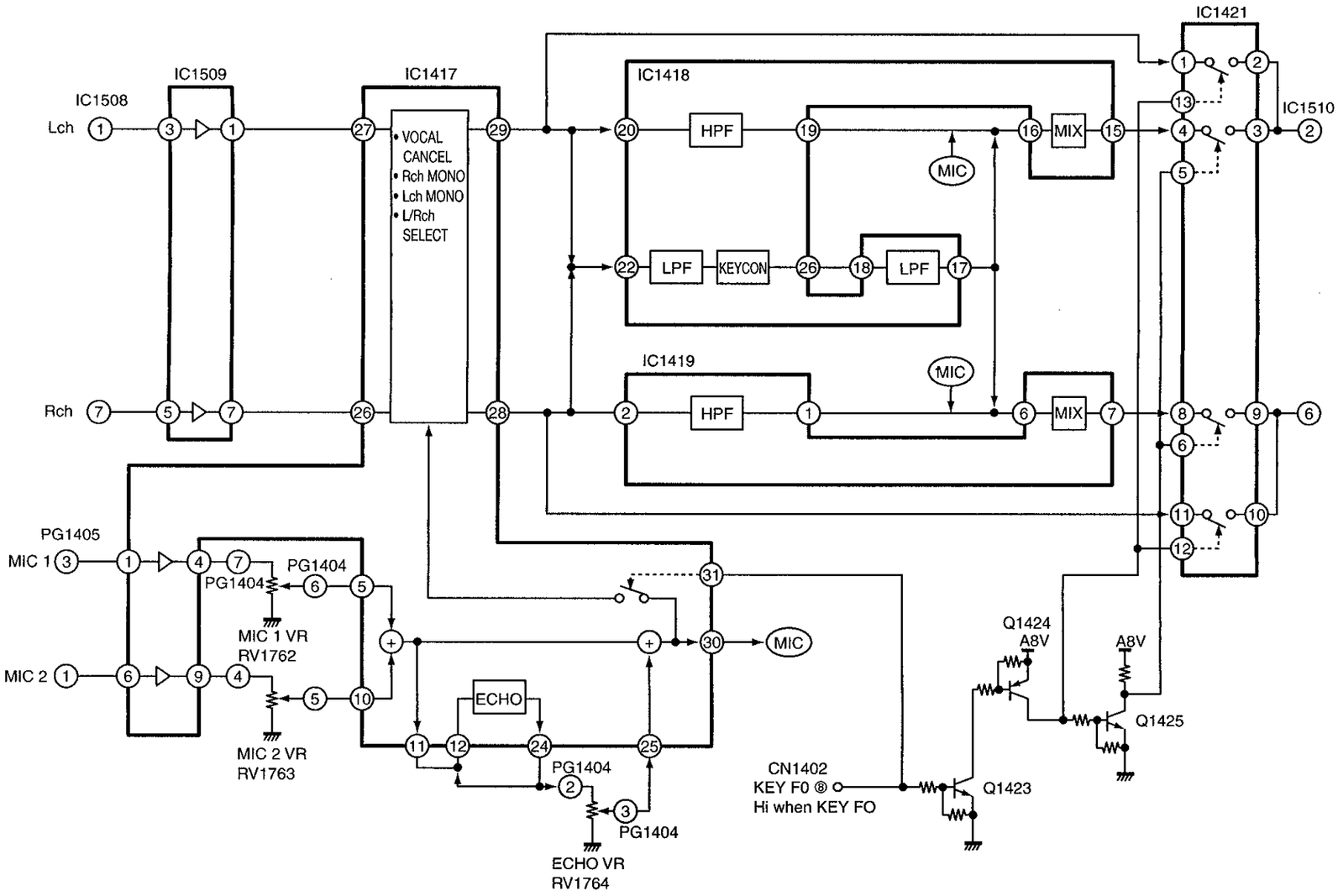


Fig. 5-5-1 KARAOKE CIRCUIT (KEYCON ALTERNATIVE CIRCUIT included.)

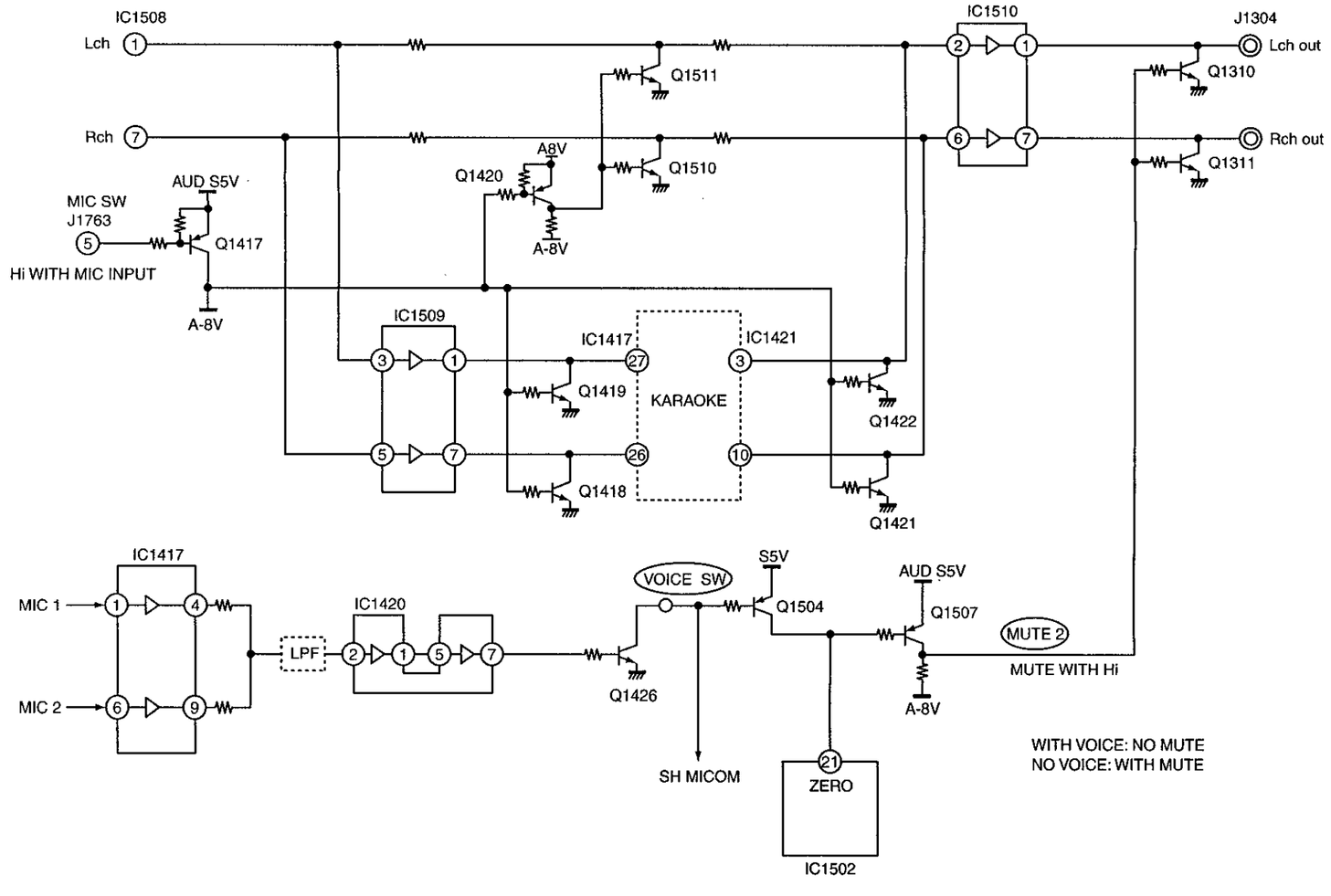


Fig. 5-5-2 KARAOKE CIRCUIT/VOICE SW

5-6 FRONT (FSW) SUBSTRATE CIRCUIT

(1) FL MICOM (IC1701)

It performs communications with SH MICOM (⑥, ⑦, ⑩ ~ ⑬, ⑲, ㉕ pins), including the main frame KEY and remote control operation, FL tube (IC1702) drive, and lighting of power indicator. In addition, it works also in standby mode. When power is 'ON', it outputs control signal at ㉝ pin to start all power sources and voltages and unlock short circuit toward GND of SH MICOM reset IC (IC1605) output.

(2) INCLUSION OF MAIN FRAME KEY AND REMOTE CONTROL OPERATION

Input is done to FL MICOM at ②~④ pins for operation of S1701 ~ S1715 and S1761 ~ S1763 of mainframe KEY. Input is done to FL MICOM at ㉓, ㉔, ㊲~㊵ pins for JOG SHUTTLE SW (S1718) operation.

Remote control signal is received by ultra-red receiver element (IC1703), output at ① pin and input to FL MICOM at ㉖ pin.

(3) FL TUBE DRIVE

Grid voltage of FL TUBE at ㉝~㊳ pins is controlled from FL MICOM ㊶~㊻ PINS; anode voltage of FL TUBE at ⑤~㉒ pins from FL MICOM ㊶~㊾ pins. Among which FL MICOM 65~69 pins are connected to A-20V by R1743~R1743 because no pull down resistance is built-in in IC.

Filament voltage (AC4.2V) is supplied from power source to FL TUBE at ①, ②, ㊶, ㊷ pins.

(4) POWER INDICATOR

Control signal output from FL MICOM ㉞, ㉟ pins puts LED driving transistors Q1703 and Q1704 'ON' or 'OFF' then lights 2-color LED (LED1761) green or red. When power is 'ON', Q1704 is 'ON' and lighted green; when standby, Q1703 is 'ON' and lighted red.

5-7 POWER SUPPLY CIRCUIT

(1) ESSENTIAL OF POWER SUPPLY CIRCUIT OPERATION

Fig 5-7-1 shows the block diagram of the power circuit.

Power supply is RCC switching type. Energy is stored in transformer T1, when FETQ1 is 'ON', by AC100V impressed at AC inlet. After that, when FETQ1 becomes 'OFF', the energy is released to the secondary side.

Power supply to diverse circuits from secondary side includes SW (S5V, S3.3V, S12V) that are put 'ON' by FL MICOM control signal (P. ON/OFF) of PG1901 ① pin and permanently 'ON' supplies (A5V, MUTE A5V, AC4.2V, A-20V, A8V, A-8V).

Detection of secondary side voltage is by A5V. D8, C16, C17 composes its secondary side commutating circuit. It is fed back by photo-coupler PHC1 to primary side and maintains stable output voltage and is supplied to FL MICOM and ultra-red reception element.

MUTE A5V is for AUDIO MUTE and supplied from A5V output.

S5V output is from A5V output and by intermediary of output control circuit Q3.

S3.3V is output from S5V at 3-terminal regulator IC2.

D11 and C24 compose secondary commutating circuit of S12 that is output by 3-terminal regulator IC3 and is for DVD ROM DRIVE use.

D11 and C24 compose secondary commutating circuits of A8V that is output by 3-terminal regulator IC4. For audio circuit proper +5V power supply, AUD S5V is produced from A8V in 5V regulator IC1506 (in DEC substrate).

D13 and C29 compose secondary commutating circuit of A-8V and it output -8V by transistor Q7 and Zener diode D20.

A-20V is negative power supply to FL tube. D14 and C33 compose its secondary commutating circuit and output -20V by transistor Q6 and Zener diode D17.

AC4.2V is for FL tube heater. To prevent fluctuation of output voltage due to that of power source, a self-exciting push-pull circuit is used. It is input from A5V, passes DC/AC inverter composed of transistors Q8, Q9, and transformer T2 and output. It supplies stable voltage without being disturbed by power source fluctuations. It plays an important role in FL tube life maintenance and against brightness decrease

(2) OPERATION OF PROTECTION CIRCUIT

PROTECTION CIRCUITS are different according to different power supplies.

For A5V and S5V,when load current increases and exceeds the control limit of the primary side of the regulator, the over current protection circuit of the primary side operates and regulator output will decrease suddenly. At the same time other outputs stop.

For S12V, S3.3V, and A8V, when load current increases and exceeds the control limit of 3-terminal regulator, the internal over current protection circuit operates and output will decrease suddenly.

Pulling the plug from the wall socket eliminates a short circuit and plugging in again restores the normal state.

When A-8V or A-20V output is short circuited, fuse F2 will open to protect circuit. When AC4.2V output is short circuited, fuse F3 will open to protect the circuit. When this and A5V are short circuited, fuse resistance R26 and R27 will open to protect the circuit.

For over current protection for A5V, destruction of Zener diode by short will stop output. The circuit is protected in this way.

By pulling off plug from wall socket, eliminating short circuit, replace destroyed parts, and plug in again, the normal state will be restored.

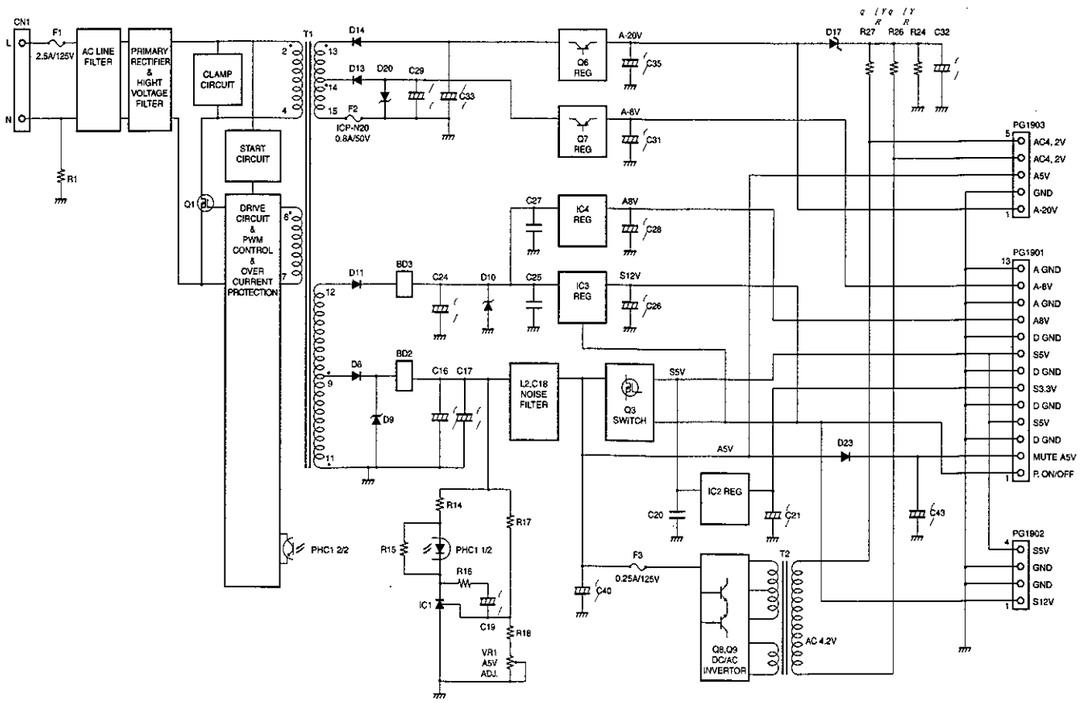


Fig. 5-7-1 BLOCK DIAGRAM OF POWER SUPPLY CIRCUITS

5-8 CLOCK CIRCUITS

5-8-1 27MHzX'TAL (X2201)

Block diagram f 27 MHz clock circuit is shown in Fig. 5-8-1.

When power is supplied to 27 MHz X'TAL, it generates 27MHz clock and input it to A/V DECODER (IC1201, VIDEO ENCODER (IC2202), and PLL (IC1504).

(1) A/V DECODER

At A/V DECODER it is used as CLOCK VCK (input at (106) pin) of VIDEO INTERFACE signal and output digital video stream synchronized to VCK from 8bit video data bus VDATA[7:0] (output at (108) ~ (110), (112), (114), (116) ~ (118) pins)

(2) VIDEO ENCODER

At VIDEO ENCODER it is used as SYSTEM CLOCK CLK (input at ㊸ pin) and output horizontal synchronous $\overline{\text{HSYNC}}$ (output at ㊾ pin) and vertical synchronous $\overline{\text{VSYNC}}$ (output at ㊿ pin) to A/V DECODER.

(3) PLL

At PLL it is used as reference signal that generates audio external frequency clock signal DA-XCK (output at ② pin).DA-XCK IS supplied to A/V DECODER (input at (121) pin) and Audio DAC (input at IC1502 ⑤ pin). The former is used as exterior clock that generates Audio bit clock DA-BCK (output at (126) pin) and LR clock DA-LRCK (output at (125) pin); the latter is used as System clock.

DA-XCK	Is external clock used for generating DA-BCK and DA-LRCK. DA-XCK takes frequency 384 times the sampling frequency.
DA-BCK	Is Audio bit clock obtained by dividing DA-XCK in 8 equal parts. It takes frequency 48 times that of sampling.
DA-LRCK	Is clock that identifies channel (Lch or Rch) against all Audio sampling.

* The Audio Interface Unit inside A/V DECODER corresponds to sampling frequencies (fs) 44.1kHz (CD-DA, Video-CD), 48kHz, 96kHz (DVD).

The frequency of DA-BCK is defined by Formula 5-8-1:

$f_{DA\text{-}BCK}$ = Audio data bit length * 2 * fs 5-8-1

At A/V DECODER, input to DA-XCK is divided into 8 equal parts and output as DA-BCK (Formula 5-8-2)

$f_{DA\text{-}BCK} = f_{DA\text{-}XCK} / 8$ 5-8-2

Therefore, DA-XCX frequency takes the value 384fs according to formulas 5-8-1 and 5-8-2. Audio data bit length is fixed 24bit. (Formula 5-8-3)

$f_{DA\text{-}XCX}$ = Audio data bit length * 2 * fs * 8 = 384fs 5-8-3

According to Formulas 5-8-2 and 5-8-3, A/V DECODER drives DA-BCK with frequency 48 times of sampling frequency. (Formula 5-8-4)

$f_{DA\text{-}BCK}$ =384fs/8 = 48fs 5-8-4

The relationships between Audio interface signals (DA-XCK, DA-LRCK, DA-BCK) and each sampling frequency are as follows:

◎ Sampling frequency: 44.1 kHz (FOR CD-DA AND Video-CD)

DA-XCK 384*fs=16.934MHz
DZ-BCK DA-XCK/8=2.1168MHz
DA-LRCK DA-BCK/48=44.1kHz=fs

◎ Sampling frequency: 48kHz (for DVD)

DA-XCK 384*fs=18.432MHz
DA-BCK DA-XCK/8=2.304MHz
DA-LRCK DA-BCK/48=48kHz=fs

◎ Sampling frequency: 96kHz (for DVD)

DA-XCK 384*fs=36.864MHz
DA-BCK DA-XCK/8=4.608MHz
DA-LRCK DA-BCK/48=96kHz=fs

5-8-2 30MHzX'TAL (X2202)

30 MHzX'TAL (X2202), the same as 27 MHzX'TAL, generates 30 MHz clock by supplying power. It is used as signal for generating A/V DECODER system clock.

From input SYCCLK (IC1201 (152) PIN) it generates inside the IC an internal 90MHz clock and is used as an interior processor as well as system clock for internal operations.

5-8-3 20MHzX'TAL (X1601)

20MHz clock is generated by attaching 20MHz crystal trembler to SH MICOM (IC1601) and used as the system clock of SH MICOM. This system clock is supplied to I/F GATE ARRAY (input at IC1101 ㊴ pin) and used as clock.

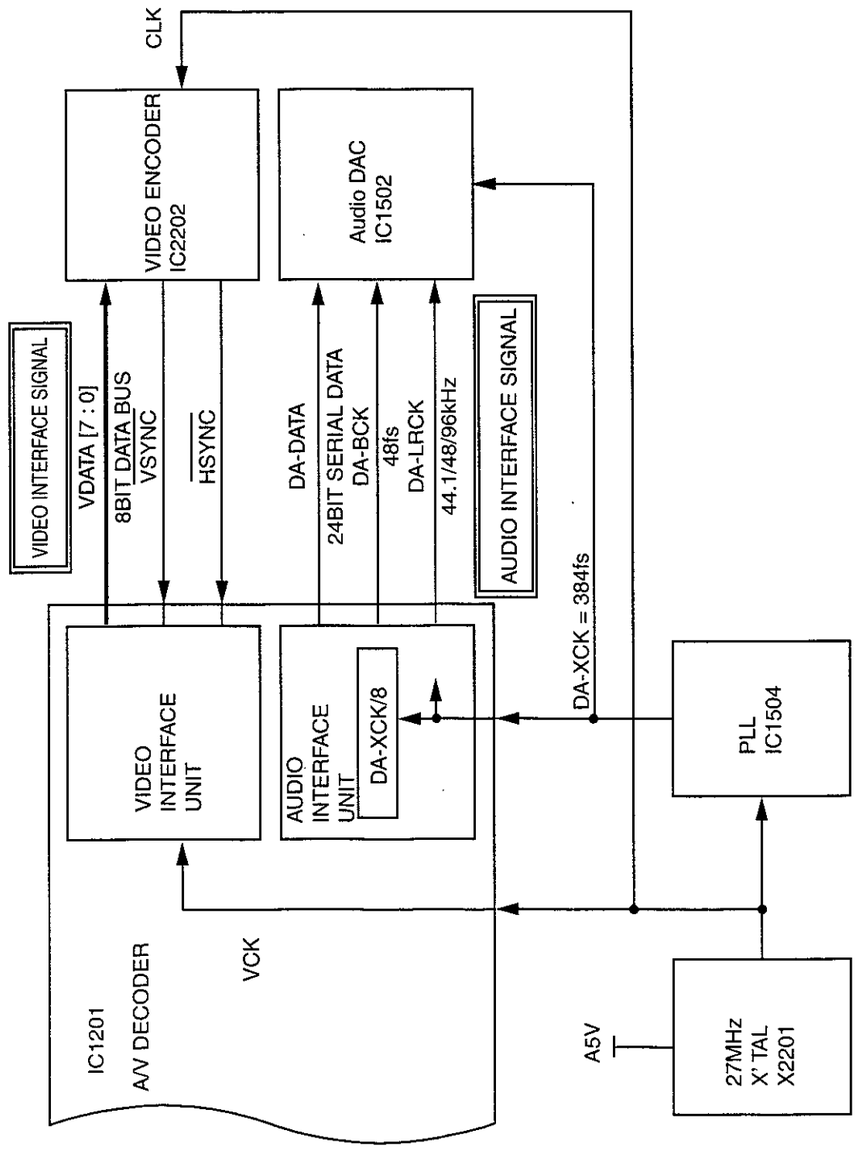


Fig. 5-8-1 BLOCK DIAGRAM OF 27MHz CLOCK CIRCUITS

6. SERVICE POINTS

6-1 TO REMOVE TOP COVER

The top cover is fastened on the front panel with 4 clicks.

1. Disengage outside clicks and clicks ① and ④.
(1) Lift the rear of the top cover about 15° as shown by Arrows A.
(2) Lift both sides of the front of the top cover in the direction shown by Arrows B and disengage clicks ① and ④.
2. Disengage inside clicks and clicks ② and ③.
(1) After the above operations in 1, lift more and deform both sides of the front of the top cover along Arrows B to disengage clicks ② and ③.
(2) To facilitate the operation, you can do it in small steps.

< Caution >
Clicks on the front panel may be damaged if you lift the rear of the top cover by more than 20°.

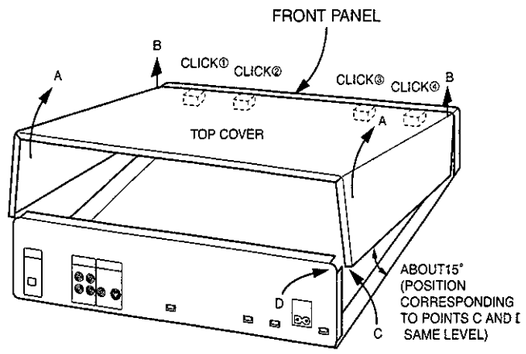


Fig. 6-1 DISASSEMBLING OF TOP COVER

6-2 TO REINSTALL TOP COVER

Keep the top cover at about 15¢Xinclination and engage it to the front panel clicks.

1. At this point, lift more and deform both sides of the front of the top cover along Arrows B to engage clicks ② and ③.
2. Stop the deformation and engage outside clicks and clicks ① and ④.

< Caution >
The front cover edge may be damaged if you let E of the top cover ride edge F of the front panel while reinstalling the top cover.

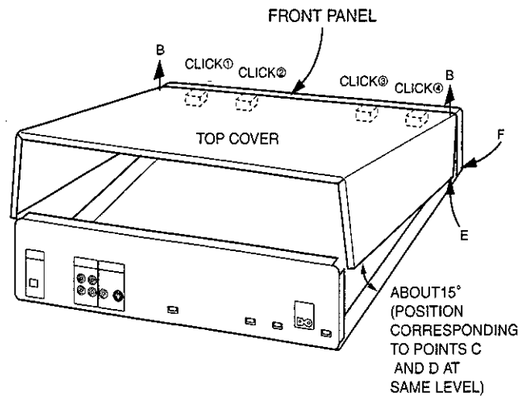
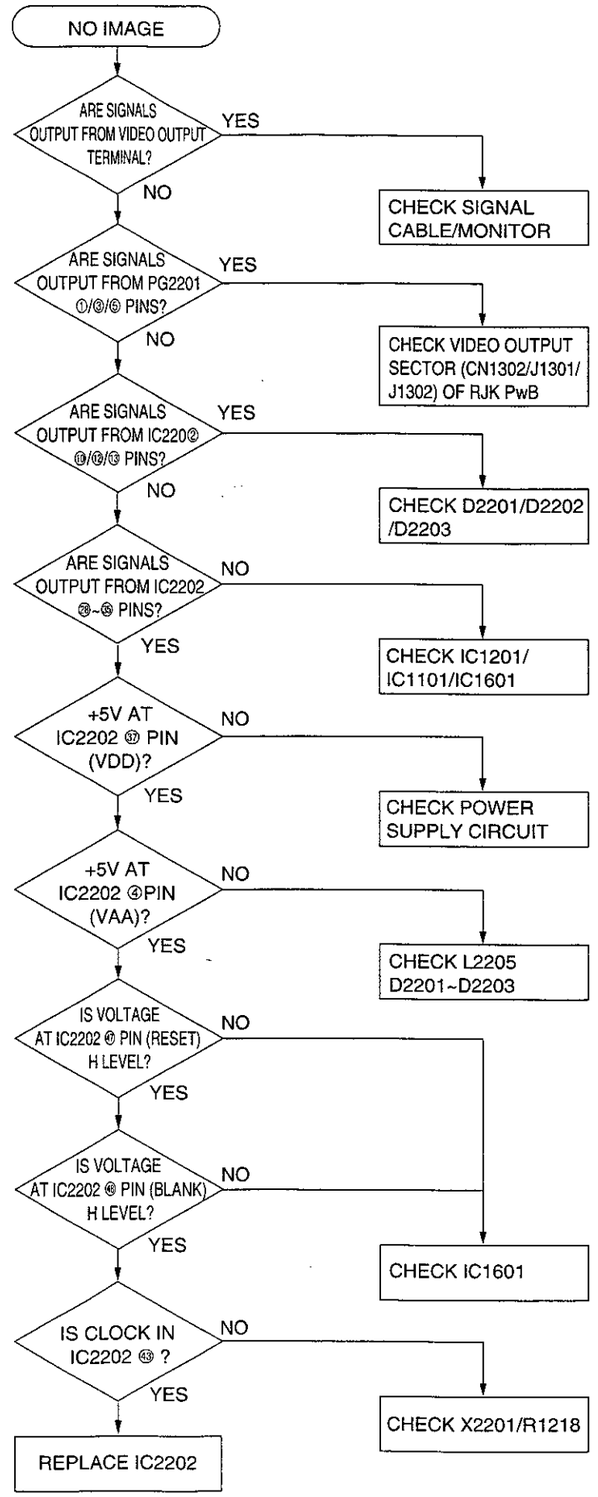


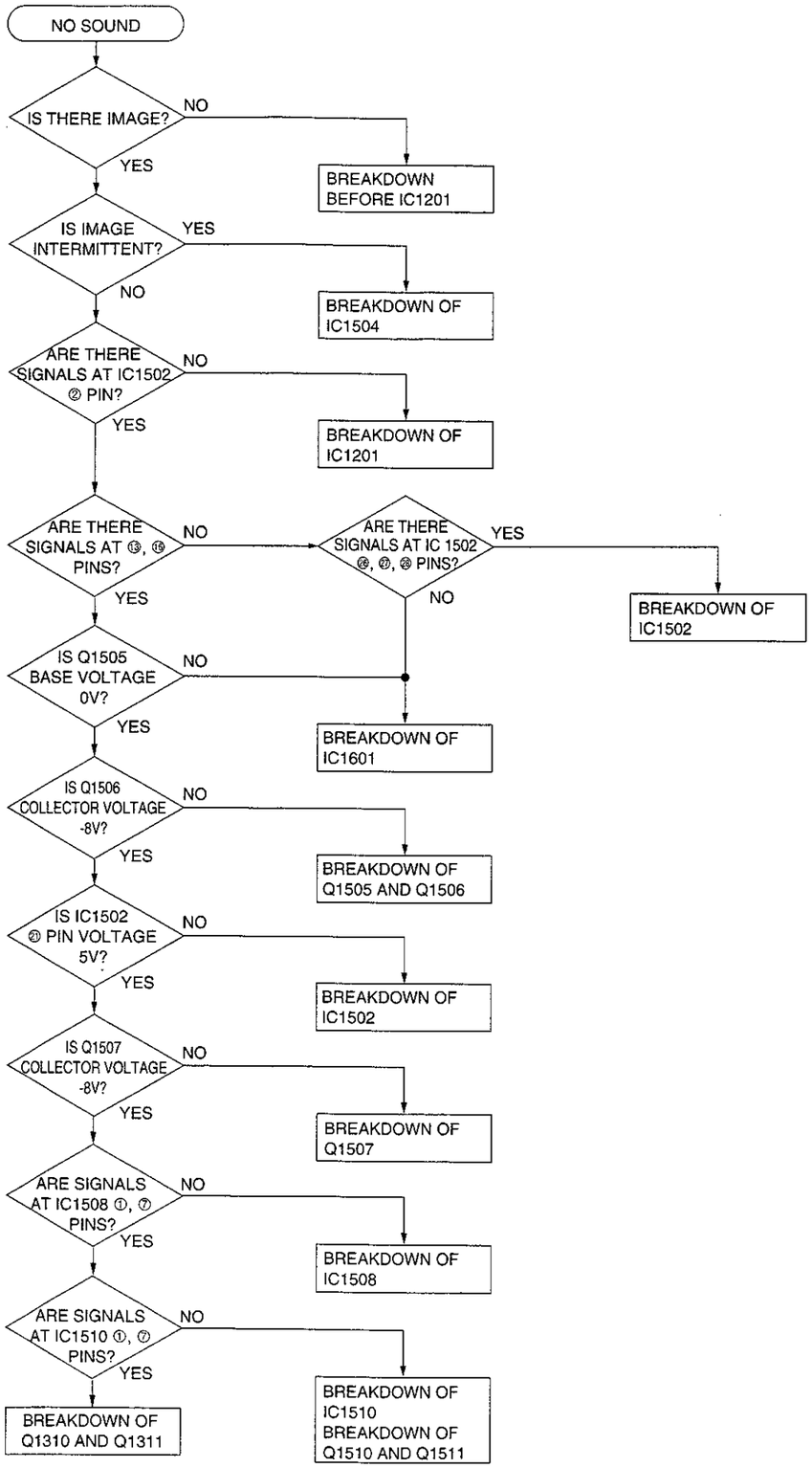
Fig. 6-2 REINSTALLING OF TOP COVE

7. TROUBLE SHOOTING

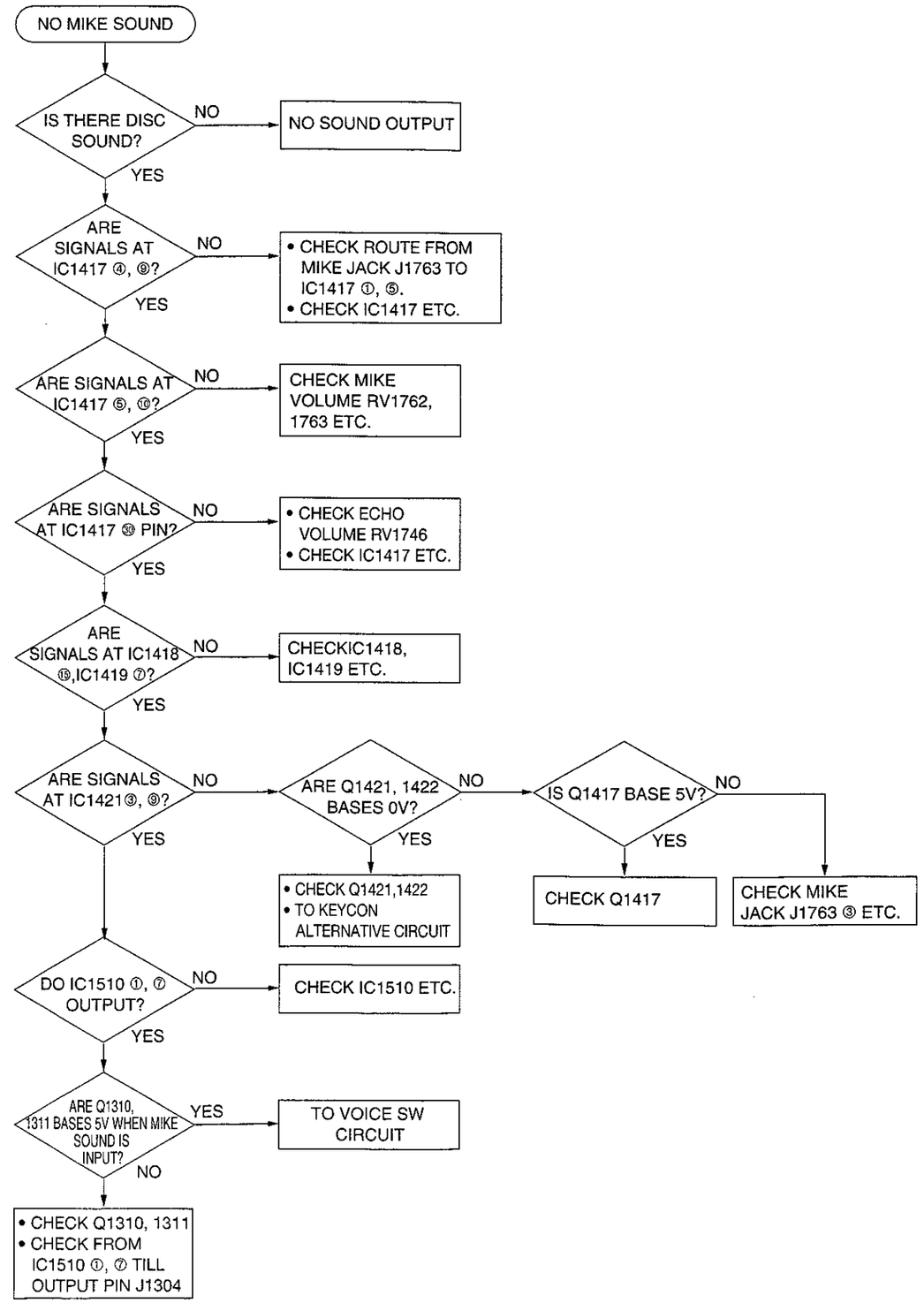
7-1 VIDEO CIRCUIT



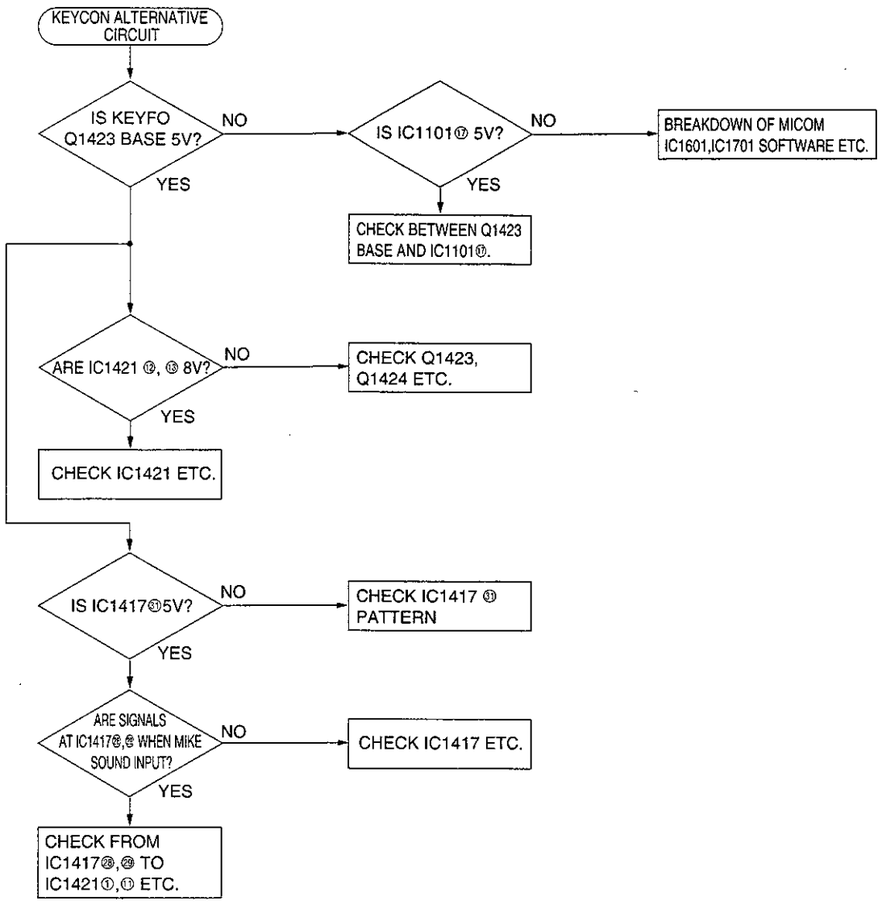
7-2 AUDIO CIRCUIT



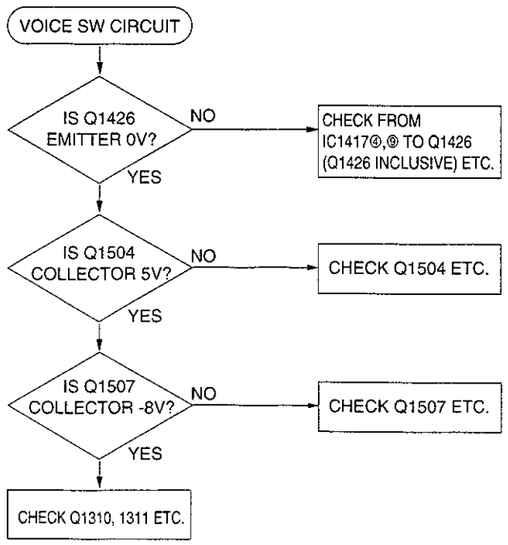
7-3 KARAOKE CIRCUIT



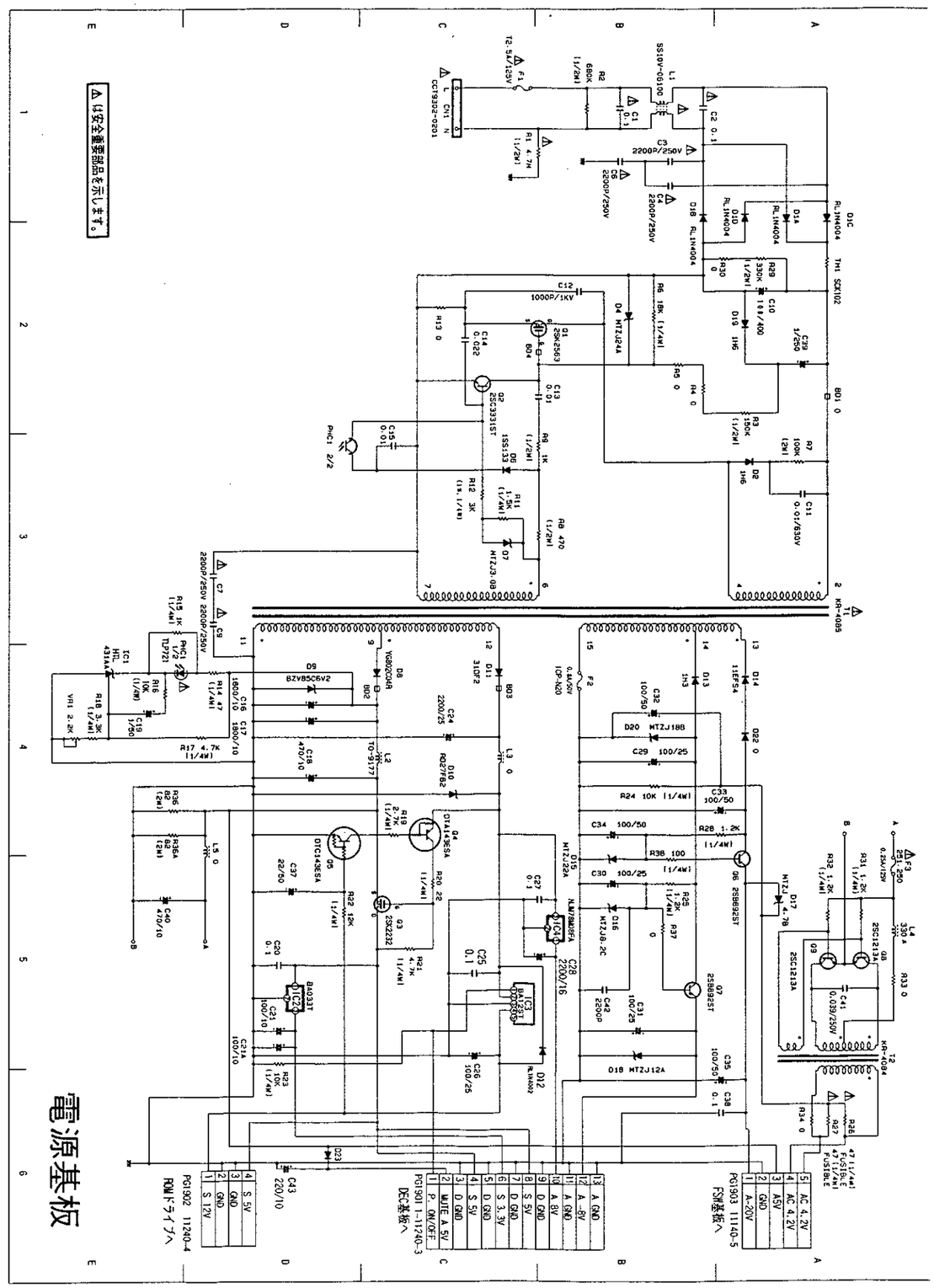
7-4 KEYCON ALTERNATIVE CIRCUIT (KEY CONTROL PRESET AT CENTER)



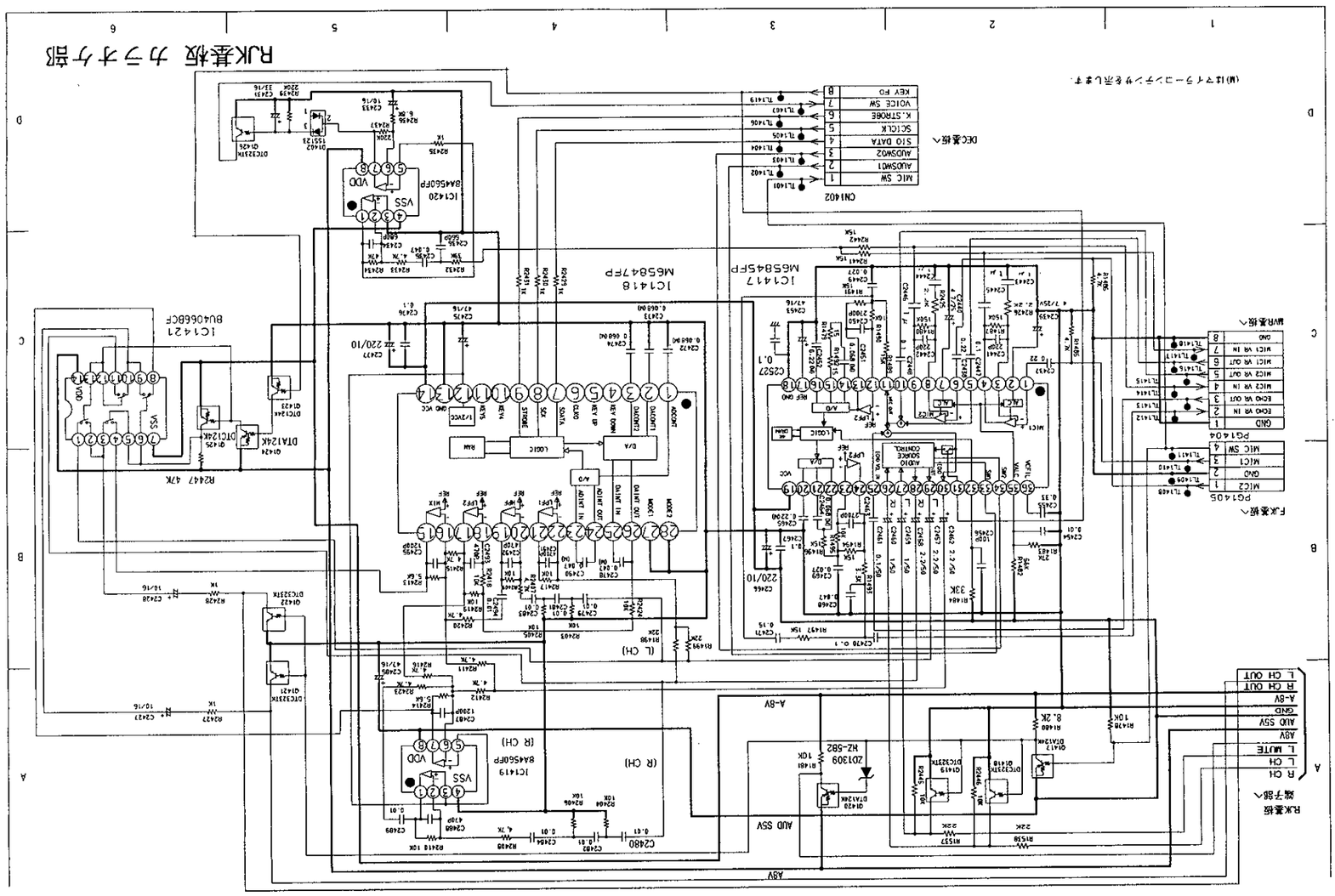
7-5 VOICE SW CIRCUIT The following is in case of mike sound input.



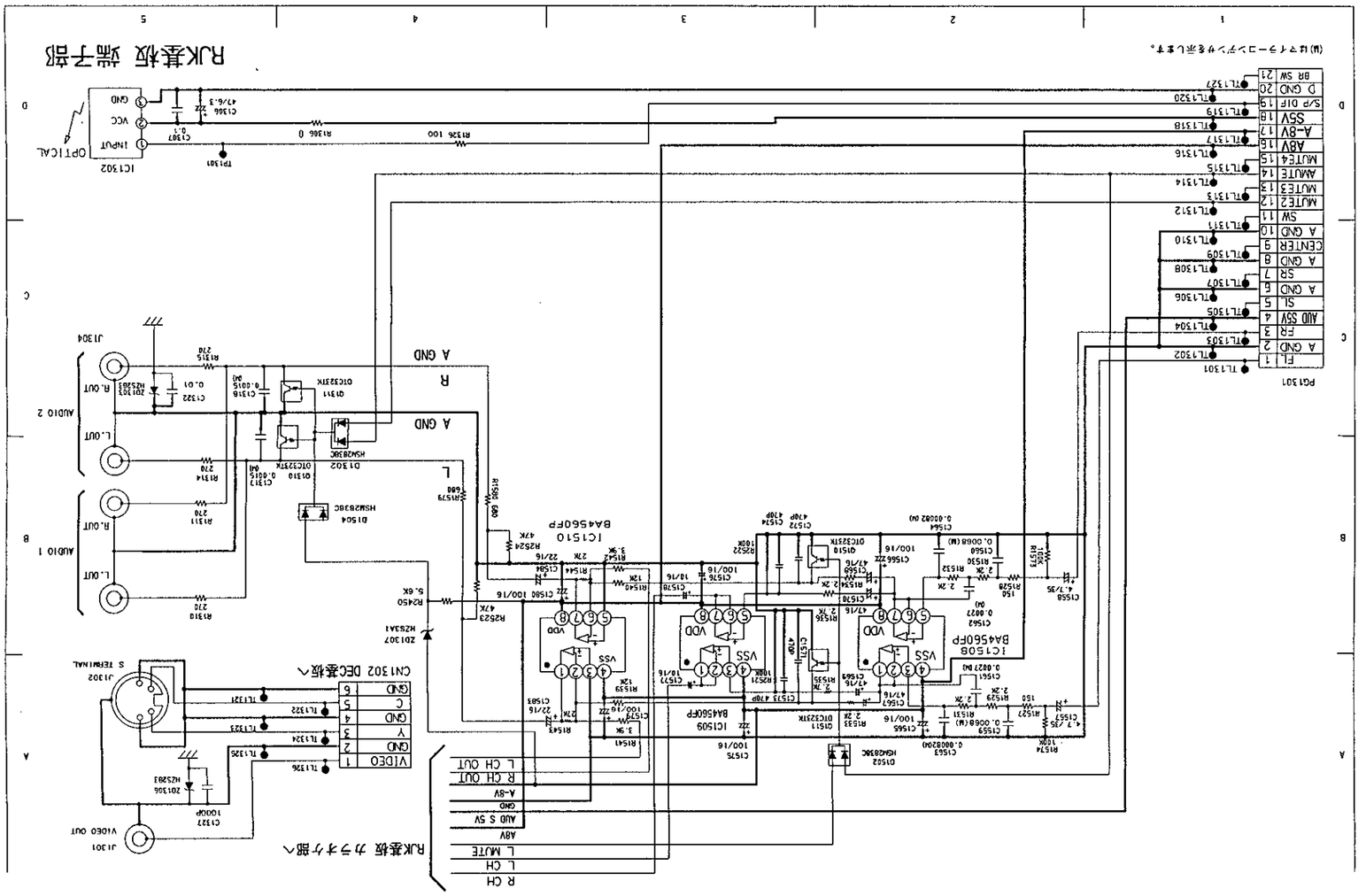
8. 基本回路図

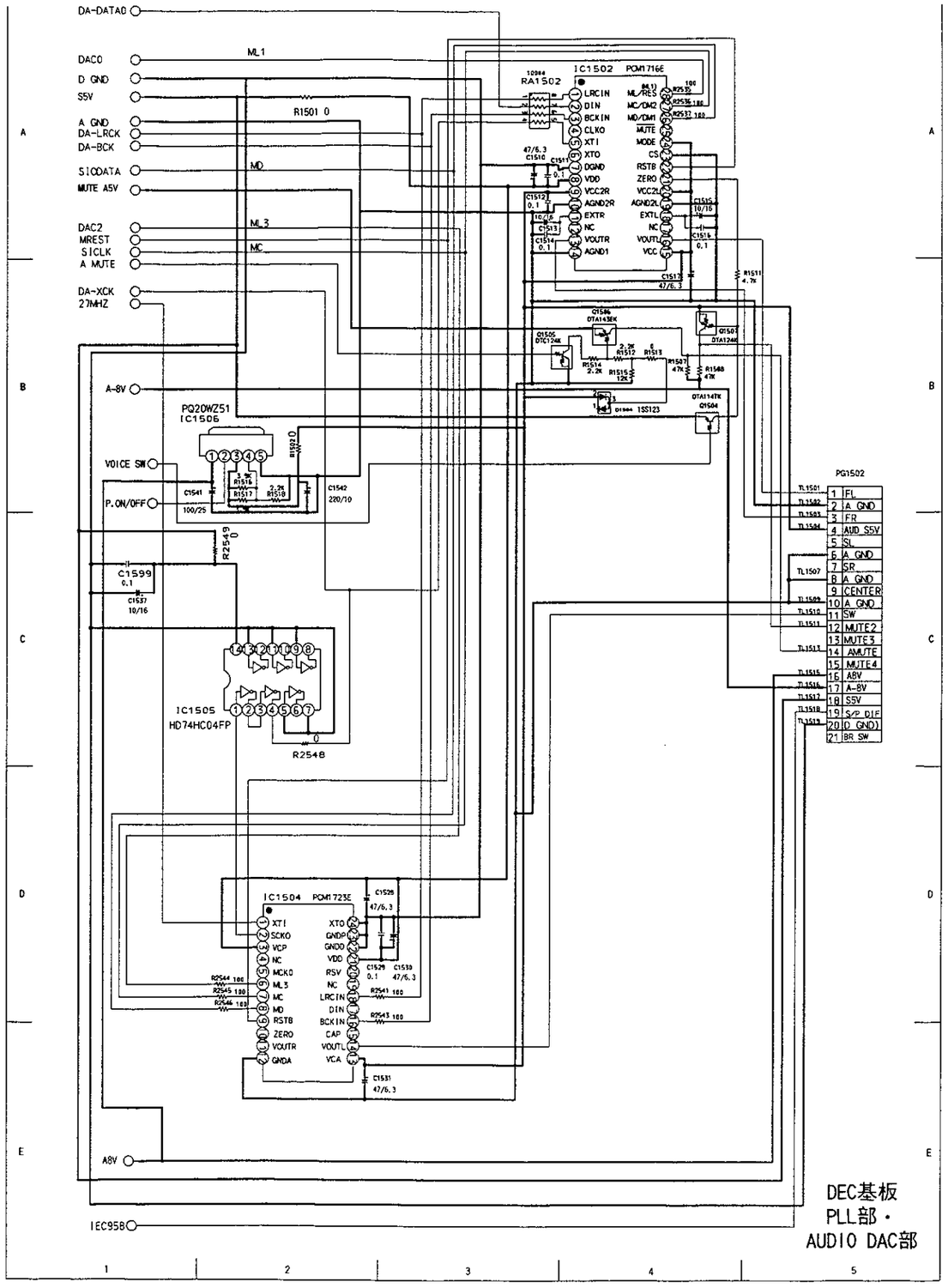


RJK基板 ケミカル部



RJK基板 端子部





DEC基板
PLL部・
AUDIO DAC部

DEC基板
AVデコーダ部
ビデオエンコーダ部 へ

DEC基板　AVデコーダ部・ビデオエンコーダ部 へ

DEC基板 I/Fゲートアレイ部へ

DEC基板 PLL部・AUDIO DAC部へ

DEC基板 SHマイコン部

IC1601
SH7020

IC1603
HM5142650J-6

IC1605
RN5VS45AA

IC1606 HD74HC14FP-T

IC1602
AT49F4096-90TC

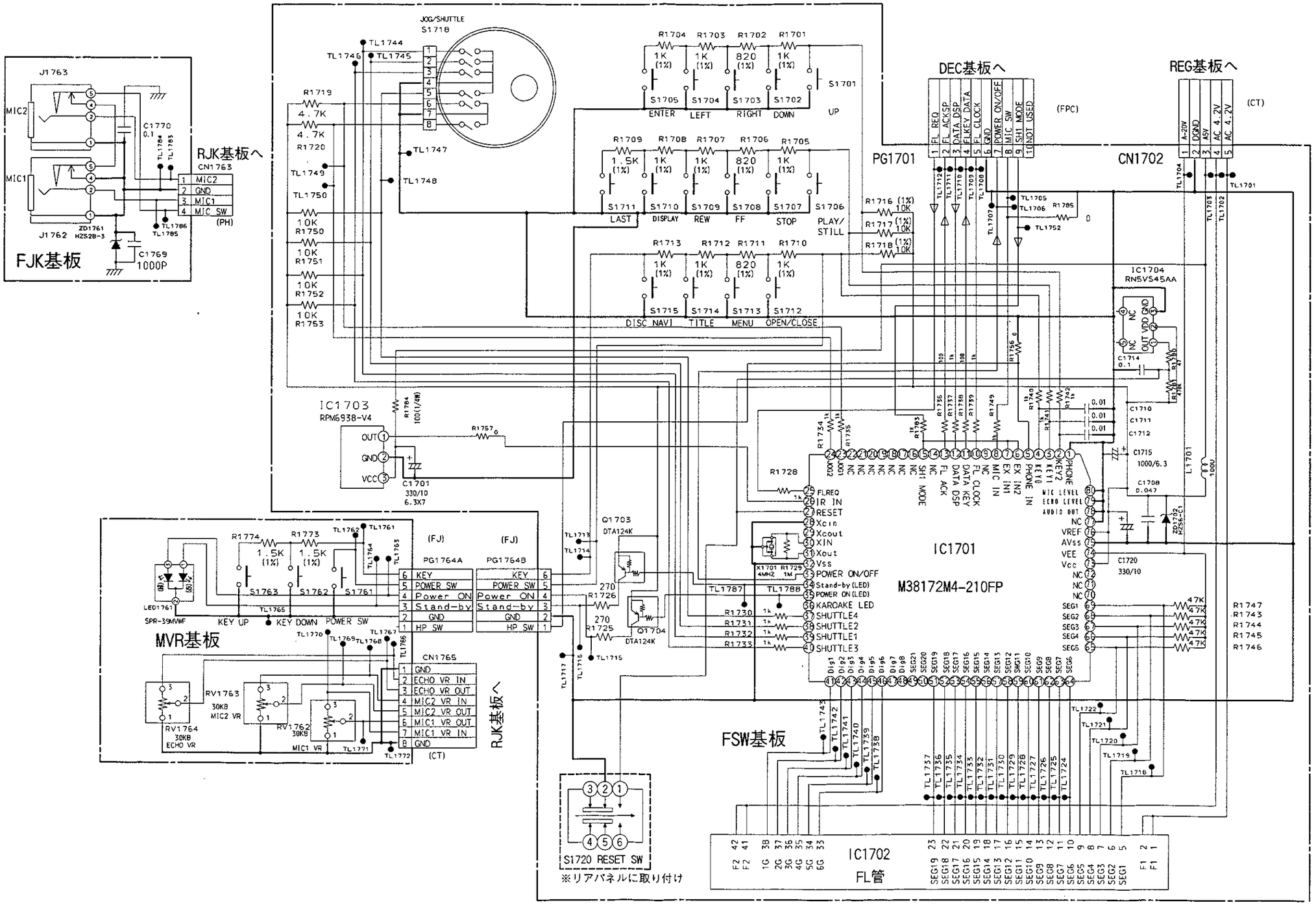
AT24C16N-10SC

MIC SW

P.ON/OFF
MREST
D GND
DAC0
DAC1
DAC2
A MUTE
27MHZ
DA-DATA0
DA-DATA1
DA-DATA2
DA-LRCK
DA-BCK
DA-XCK
LFE
AC3
VOICE SW
SICLK
SIODATA
PG1601 TO RJK

1	MIC SW
2	AUDSW01
3	AUDSW02
4	SIODATA
5	SCICLK
6	K.STROBE
7	VOICE SW
8	KEYF0

FSW基板・FJK基板・MVR基板



DEC基板 SHマイコン部へ

PG1201

13	A GND
12	A-8V
11	A GND
10	A8V
9	D GND
8	S5V
7	D GND
6	S3.3V
5	D GND
4	S5V
3	D GND
2	A5V
1	P. ON/OFF

C2231 0.1

L1202 LCFビーズ5VT TL1204

C2232 470/10

C2233 470/10

TL1208 TL1206 TL1202

TL1207

TL1203 TL1201

TL1205

A5V
S5V
A8V
A GND
A-8V

DEC基板 PLL部・AUD10 DAC部へ

L1203 LCFビーズ5VT

C1216 100/10

C1215 0.1 CK

C1218 0.1 CK

X2202 30MHz-XTAL

30MHz

C1219 0.1 CK

X2201 OSX270X12(I)HC-4

27Mz

R1237 47

R1218 47

R1219 47

R1238 47

C1240 0.1 CK

IC1202 HD74LS32FP

1A 1B 1Y 2A 2B 2Y GND
VCC 4A 4B 4Y 3A 3B 3Y

CS6

ZWAIT

R3281 0

R4221 5.6K

R3282 4.7K

C1214 100P CK

C1231 0.1

C1232 0.1

C1233 0.1

C1234 0.1

C1235 0.1

C1203 0.1 CK

C1202 0.1 CK

C1201 100/10

L1201 LCFビーズ5VT

C1236 0.1

C1221 0.1

C1222 0.1

C1223 0.1

C1224 0.1

ZRES SD0 SD1 SD2 SD3 SD4 SD5 SD6 SD7 INT AVDEC ZRD ZWR GCUBECS SA0 SA1 SA2

R1221 47 R1222 47 R1223 47 R1224 47 R1225 47 R1226 47 R1227 47 R1228 47 R1229 1K R1230 47 R1231 47 R1232 2.2K R1233 0 R1234 0 R1235 0 R1236 0

HDATA1 VDD NC HDATA2 HDATA3 HDATA4 NC HDATA5 VSS HDATA6 NC HDATA7 SWAIT INT AVDEC RD1 NC WRL A_VDD CS4DN NC A_VSS SA0 SA1 NC SA2

MDATA63 MDATA62 MDATA61 MDATA60 MDATA59 MDATA58 MDATA57 MDATA56 MDATA55 MDATA54 MDATA53 MDATA52 MDATA51 MDATA50 MDATA49 MDATA48 MDATA47

ERROR NC DACK CSTROBE REQUEST NC VSS DVD7 VSS DVD6 NC VDD DVD5 VDD5MAX NC DVD4 DVD3 DVD2 NC VDD DVD1 DVD0 IEC958 DA-XCK DA-BCK DA-LRCK DA-DATA1 DA-DATA0 VSS NC HSYNC NC VSYNC VDATA7 VDATA6 VDATA5 NC VDATA4 VDD VDATA3 NC VDATA2

CSTROBE REQUEST DVD7 DVD6 DVD5 DVD4 DVD3 DVD2 DVD1 DVD0 DA-DATA2 DA-XCK DA-BCK DA-LRCK DA-DATA1 DA-DATA0

VDATA7 VDATA6 VDATA5 VDATA4 VDATA3 VDATA2 VDATA1 VDATA0

R1201 R1202 R1203 R1204 R1205 R1206 R1207 R1208 R1209 R1210 R1211 R1212 R1213 R1214 R1215 R1216 R1217

MDATA43 MDATA42 MDATA41 MDATA40 MDATA39 MDATA38 MDATA37 MDATA36 MDATA35 MDATA34 MDATA33 MDATA32 MDATA31 MDATA30 MDATA29 MDATA28 MDATA27 MDATA26 MDATA25 MDATA24 MDATA23 MDATA22 MDATA21 MDATA20 MDATA19 MDATA18 MDATA17

MDATA46 MDATA45 MDATA44

NC VSS MDATA43 MDATA42 MDATA41 NC MDATA40 MDATA39 VDD MDATA38 NC VSS MDATA37 MDATA36 NC VSS MDATA35 MDATA34 NC VDD MDATA33 MDATA32 MDATA31 NC MDATA30 MDATA29 MDATA28 NC MDATA27 MDATA26 MDATA25 NC MDATA24 VSS MDATA23 MDATA22 NC MDATA21 VDD MDATA20 NC

ZIVAD6-C IC1201

(52) SYSCK (53) NC (54) NC (55) RESET (56) HDATA0

(04) VSS (05) VCK (01) NC (08) VDATA0 (09) VDATA1

(1) VDD (2) MDATA46 (3) NC (4) VSS (5) MDATA45 (6) MDATA44

(42) MDATA19 (43) MDATA18 (44) MDATA17 (45) NC (46) MDATA16 (52) MCE

DEC基板 I/Fゲートアレイ部へ

DEC基板 SHマイコン部へ

DEC基板 SHマイコン部へ

DEC基板 I/Fゲートアレイ部へ

A B C D

板　I/Fゲートアレイ部へ

13	A GND
12	A-8V
11	A GND
10	A8V
9	D GND
8	S5V
7	D GND
6	S3.3V
5	D GND
4	S5V
3	D GND
2	A5V
1	P. ON/OFF

PG1201

DEC基板
PLL部・AUDIO DAC部へ

DEC基板 SHマイコン部へ

DEC基板 SHマイコン部へ

AD6-C

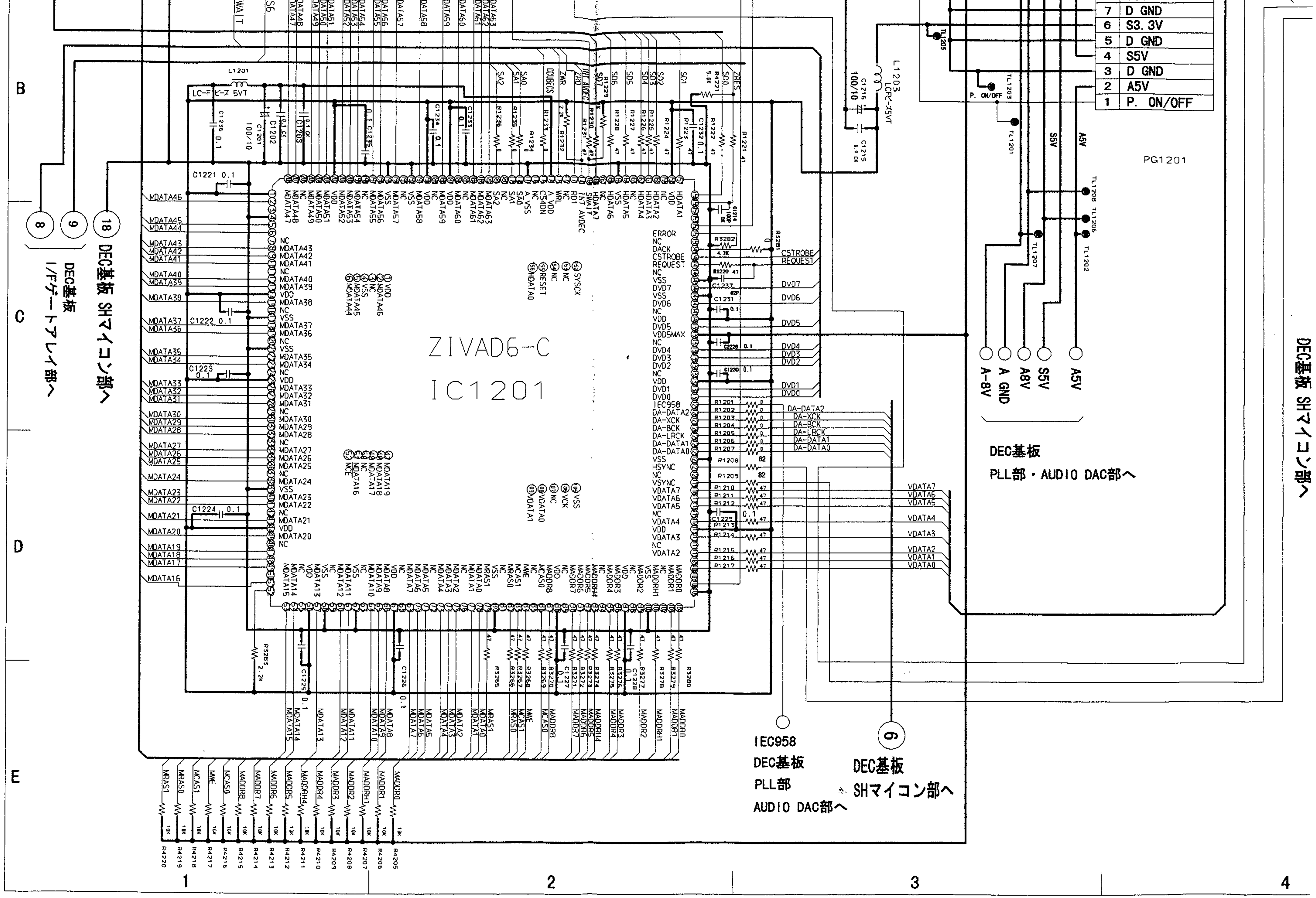
1201

A

B

C

D


ZIVAD6-C
IC1201
DEC基板 SHマイコン部へ
DEC基板 I/Fゲートアレイ部へ
DEC基板 PLL部・AUDIO DAC部へ
IEC958 DEC基板 PLL部 AUDIO DAC部へ
DEC基板 SHマイコン部へ
PG1201
7 D GND
6 S3.3V
5 D GND
4 S5V
3 D GND
2 A5V
1 P. ON/OFF
A-8V
A GND
A8V
S5V
A5V
L1201
L1203
LC-F ビーズ 5VT
CSTROBE
REQUEST
DVD7
DVD6
DVD5
DVD4
DVD3
DVD2
DVD1
DVD0
DA-DATA2
DA-XCK
DA-BCK
DA-LRCK
DA-DATA1
DA-DATA0
VDATA7
VDATA6
VDATA5
VDATA4
VDATA3
VDATA2
VDATA1
VDATA0
B
C
D
E
1
2
3
4

7	D GND
6	S3.3V
5	D GND
4	S5V
3	D GND
2	A5V
1	P. ON/OFF

PG1201

A-8V　A GND　A8V　S5V　A5V

DEC基板
PLL部・AUDIO DAC部へ

IEC958
DEC基板
PLL部
AUDIO DAC部へ

DEC基板
SHマイコン部へ

DEC基板
AVデコーダ部・ビデオエンコーダ部

PG2201
06R-FJ

1	CVBS
2	CVBSGND
3	Y
4	YGND
5	C
6	CGND

DEC基板
AVデコーダ部
ビデオエンコーダ部へ

8 9

SH 10

DEC基板 SHマイコン部へ 11

PG1103
GND 1
1Pベース付きミニプラグ

R2140-R2155
5.6K

PG1101

RESET-	1	RESET
GND	2	ATD15
DD7	3	ATD0
DD8	4	ATD14
DD6	5	ATD1
DD9	6	ATD13
DD5	7	ATD2
DD10	8	ATD12
DD4	9	ATD3
DD11	10	ATD11
DD3	11	ATD4
DD12	12	ATD10
DD2	13	ATD5
DD13	14	ATD9
DD1	15	ATD6
DD14	16	ATD8
DD0	17	ATD7
DD15	18	
GND	19	
NC	20	
DMARQ	21	DMARQ
GND	22	
DIOW-	23	DIOW
GND	24	DIOR

IC1101 UPD65625GF-114-3BA

1	ATARES		100	DVD0	
2	ATD7		99	GND	
3	ATD8		98	DVD1	
4	ATD6		97	DVD2	
5	VCC		96	DVD3	
6	LTBX (#TDI)		95	GATEST2 (VCC)	
7	ATD9		94	-MRST	
8	ATD5		93	VCC (OPEN)	
9	ATD10		92	GND (OPEN)	
10	ATD4		91	SHCLK	
11	ATD11		90	GND	
12	ATD3		89	DVD4	
13	GND		88	DVD5	
14	ATD12		87	DVD6	
15	GND (OPEN)		86	VCC	
16	ATD2		85	DVD7	
17	KARAOKE (#TMS)		84	-ZWAIT	80
18	ATD13		83	-CCUBERD	79
19	ATD1		82	-CCUBEWR	78
20	VCC		81	-CCUBECS	77
21	ATD14		80	GND	76
22	ATD0		79	AC3 (#TDO)	75
23	ATD15		78	GDREQ_SH	74
24	DMARQ ATAD		77	GDACK_SH	73
			76	ADACK_SH	72
			75	GATEST1	71
			74	-SHRD	70
			73	-SHWR	69
			72	VCC	68
			71	-SHWAIT	67
			70	GND (OPEN)	66
			69	AUDSW2 (REGWR)	65
			68	SQEZ (#TCK)	64
			67	-CS6	63
			66	-CS2	62
			65	AUDSW1 (GND)	61
			64	SA21	60
			63	SA6	59
			62	SA4	58
			61	SA3	57

RESET
ATD7
ATD8
ATD6
ATD9
ATD5
ATD10
ATD4
ATD11
ATD3
ATD12
ATD2
ATD13
ATD1
ATD14
ATD0
ATD15
DMARQ

-FRAM_WR
ADREQ_SH

REQUEST_CC
CSTROBE_CC

-CS3
-CS1

SYSCLK
INTRQ

ZWAIT
ZRD
ZWR
CCUBECS
GDREQ
GDACK
ADACK
RD
WRL
SWAIT
CS6
CS2
SA21
SA6
SA4
SA3
FRAMWR

MDATA0
MDATA1
MDATA2
MDATA3
MDATA4
MDATA5
MDATA6
MDATA7
MDATA8
MDATA9
MDATA10
MDATA11
MDATA12
MDATA13
MDATA14
MDATA15
MDATA16
MDATA17
MDATA18
MDATA19
MDATA20
MDATA21
MDATA22
MDATA23
MDATA24
MDATA25
MDATA26
MDATA27
MDATA28
MDATA29
MDATA30
MDATA31
MDATA32
MDATA33
MDATA34
MDATA35
MDATA36
MDATA37
MDATA38
MDATA39
MDATA40
MDATA41
MDATA42
MDATA43
MDATA44
MDATA45
MDATA46
MDATA47
MDATA48
MDATA49
MDATA50
MDATA51

DEC基板
AVデコーダ部
ビデオエンコーダ部 へ

8 9

10

SH

C1117 0.1

C1119 100P

SRES

SYSCLK

DVD0 DVD1 DVD2 DVD3 DVD4 DVD5 DVD6 DVD7 CSTROBE REQUEST

R1157 47 R1156 47 R1155 47 R1154 47 R2157 0 R1153 47 R1152 47 R1151 47 R1150 47 R1149 47

L2140 L2139 L2138 L2137 L2136 L2135 L2134 L2133 L2132 L2131 L2130 L2129 L2128 L2127 L2126 L2125 L2124 L2123 L2122

98 97 96 95 94 93 92 91 90 89 88 87 86 85 84 83 82 81

DVD0 GND DVD1 DVD2 DVD3 GATEST2 (VCC) -MRST VCC (OPEN) GND (OPEN) SHCLK GND DVD4 DVD5 DVD6 VCC DVD7

TDI)

-FRAM_WR
ADREQ_SH
100 99

REQUEST_CC
CSTROBE_CC
82 81

PEN)

IC1101 UPD65625GF -114-3BA

E (#TMS)

-CS1 -CS2

ATA

-ZWAIT 80
-CCUBERD 79
-CCUBEWR 78
-CCUBECS 77
GND 76
AC3 (#TDO) 75
GDREQ_SH 74
GDACK_SH 73
ADACK_SH 72
GATEST1 71
-SHRD 70
-SHWR 69
VCC 68
-SHWAIT 67
GND (OPEN) 66
AUDSW2 (REGWR) 65
SQEZ (#TCK) 64
-CS6 63
-CS2 62
AUDSW1 (GND) 61
SA21 60
SA6 59
SA4 58
SA3 57

TL2121 TL2120 TL2119 TL2118 TL2117 TL2116 TL2115 TL2114 TL2113 TL2112 TL2111 TL2110 TL2109 TL2108 TL2107 TL2106 TL2105 TL2104 TL2103 TL2102 TL2101 TL1199 TL1198 TL1197

R1148 ZRD
R1147 ZWR
R1146 CCUBECS

C1133 33P
R1145 82
R2136 R2137 47
GDREQ
5.6K GDACK
R1144 0 ADACK
R2138 5.6K
R2158 0 RD
R2159 0 WRL
C1116 0.1
R1143 47 SWAIT
C1120 33P
R2108 47
R2139 5.6K
CS6
CS2
SA21
SA6
SA4
SA3

R2121 5.6K SD0
R2122 5.6K SD1
R2123 5.6K SD2
R2124 5.6K SD3
R2125 5.6K SD4
R2126 5.6K SD5
R2127 5.6K SD6
R2128 5.6K SD7
R2129 5.6K SD8
R2130 5.6K SD9
R2131 5.6K SD10
R2132 5.6K SD11
R2133 5.6K SD12
R2134 5.6K SD13
R2135 5.6K SD14
R2136 5.6K SD15

FRAMWR

11

DEC基板 SHマイコン部へ

1
3

DEC基板
AVデコーダ部
ビデオエンコーダ部 へ

C1204 0.1 CK

R1239 10K MDATA0
R1240 10K MDATA1
R1241 10K MDATA2
R1242 10K MDATA3
R1243 10K MDATA4
R1244 10K MDATA5
R1245 10K MDATA6
R1246 10K MDATA7
R1247 10K MDATA8
R1248 10K MDATA9
R1249 10K MDATA10
R1250 10K MDATA11
R1251 10K MDATA12
R1252 10K MDATA13
R1253 10K MDATA14
R1254 10K MDATA15
R1255 10K MDATA16
R1256 10K MDATA17
R1257 10K MDATA18
R1258 10K MDATA19
R1259 10K MDATA20
R1260 10K MDATA21
R1261 10K MDATA22
R1262 10K MDATA23
R1263 10K MDATA24
R1264 10K MDATA25
R1265 10K MDATA26
R1266 10K MDATA27
R1267 10K MDATA28
R1268 10K MDATA29
R1269 10K MDATA30
R1270 10K MDATA31
R1271 10K MDATA32
R1272 10K MDATA33
R1273 10K MDATA34
R1274 10K MDATA35
R1275 10K MDATA36
R1276 10K MDATA37
R1277 10K MDATA38
R1278 10K MDATA39
R1279 10K MDATA40
R1280 10K MDATA41
R1281 10K MDATA42
R1282 10K MDATA43
R1283 10K MDATA44
R1284 10K MDATA45
R1285 10K MDATA46
R1286 10K MDATA47
R1287 10K MDATA48
R1288 10K MDATA49
R1289 10K MDATA50
R1290 10K MDATA51

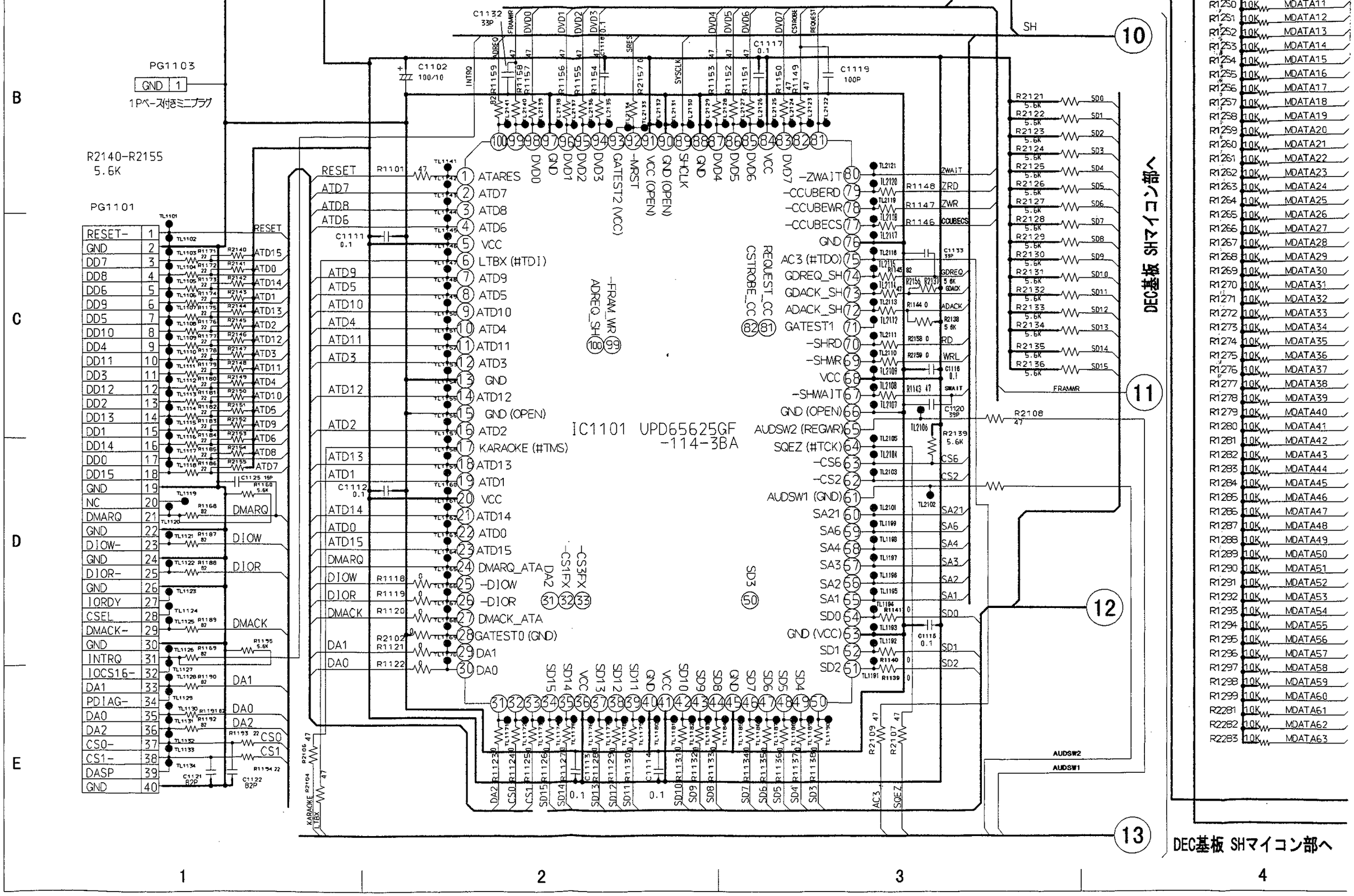
IC2203 HM514265DJ-6
IC2204 HM514265DJ-6
IC2205 HM514265DJ-6
IC2206 HM514265DJ-6

C1205 0.1 CK
C1206 0.1 CK
C1207 0.1 CK
C1208 0.1 CK
C1209 0.1 CK
C1210 0.1 CK
C1211 0.1 CK

R2284 1K
R2285 1K
R2286 1K
R2287 1K

MCAS0 MCAS1
MWE MRAS0
MADDR0 MADDR1 MADDR2 MADDR3 MADDR4 MADDR5 MADDR6 MADDR7 MADDR8
MADDRH1 MADDRH4

A B C D


PG1103
GND 1
1Pベース付きミニプラグ
R2140-R2155
5.6K
PG1101
RESET-
GND
DD7
DD8
DD6
DD9
DD5
DD10
DD4
DD11
DD3
DD12
DD2
DD13
DD1
DD14
DD0
DD15
NC
DMARQ
DIOW-
DIOR-
IORDY
CSEL
DMACK-
INTRQ
IOCS16-
DA1
PDIAG-
DA0
DA2
CS0-
CS1-
DASP
RESET
ATD15
ATD0
ATD14
ATD1
ATD13
ATD2
ATD12
ATD3
ATD11
ATD4
ATD10
ATD5
ATD9
ATD6
ATD8
ATD7
DMARQ
DIOW
DIOR
DMACK
DA1
DA0
DA2
CS0
CS1
R1101
ATARES
ATD7
ATD8
ATD6
VCC
LTBX (#TDI)
ATD9
ATD5
ATD10
ATD4
ATD11
ATD3
GND
ATD12
GND (OPEN)
ATD2
KARAOKE (#TMS)
ATD13
ATD1
VCC
ATD14
ATD0
ATD15
DMARQ_ATA
-DIOW
-DIOR
DMACK_ATA
GATEST0 (GND)
DA1
DA0
IC1101 UPD65625GF
-114-3BA
-ZWAIT
-CCUBERD
-CCUBEWR
-CCUBECS
GND
AC3 (#TDO)
GDREQ_SH
GDACK_SH
ADACK_SH
GATEST1
-SHRD
-SHWR
VCC
-SHWAIT
GND (OPEN)
AUDSW2 (REGWR)
SQEZ (#TCK)
-CS6
-CS2
AUDSW1 (GND)
SA21
SA6
SA4
SA3
SA2
SA1
SD0
GND (VCC)
SD1
SD2
ZWAIT
ZRD
ZWR
CCUBECS
GDREQ
GDACK
ADACK
RD
WRL
SWAIT
FRAMWR
CS6
CS2
SA21
SA6
SA4
SA3
SA2
SA1
SD0
SD1
SD2
AUDSW2
AUDSW1
SH
DEC基板 SHマイコン部へ
DEC基板 SHマイコン部へ
10
11
12
13

DEC基板 SHマイコン部へ

IC1101 UPD65625GF -114-3BA

DEC基板 SHマイコン部へ

DEC基板 I/Fゲートアレイ部

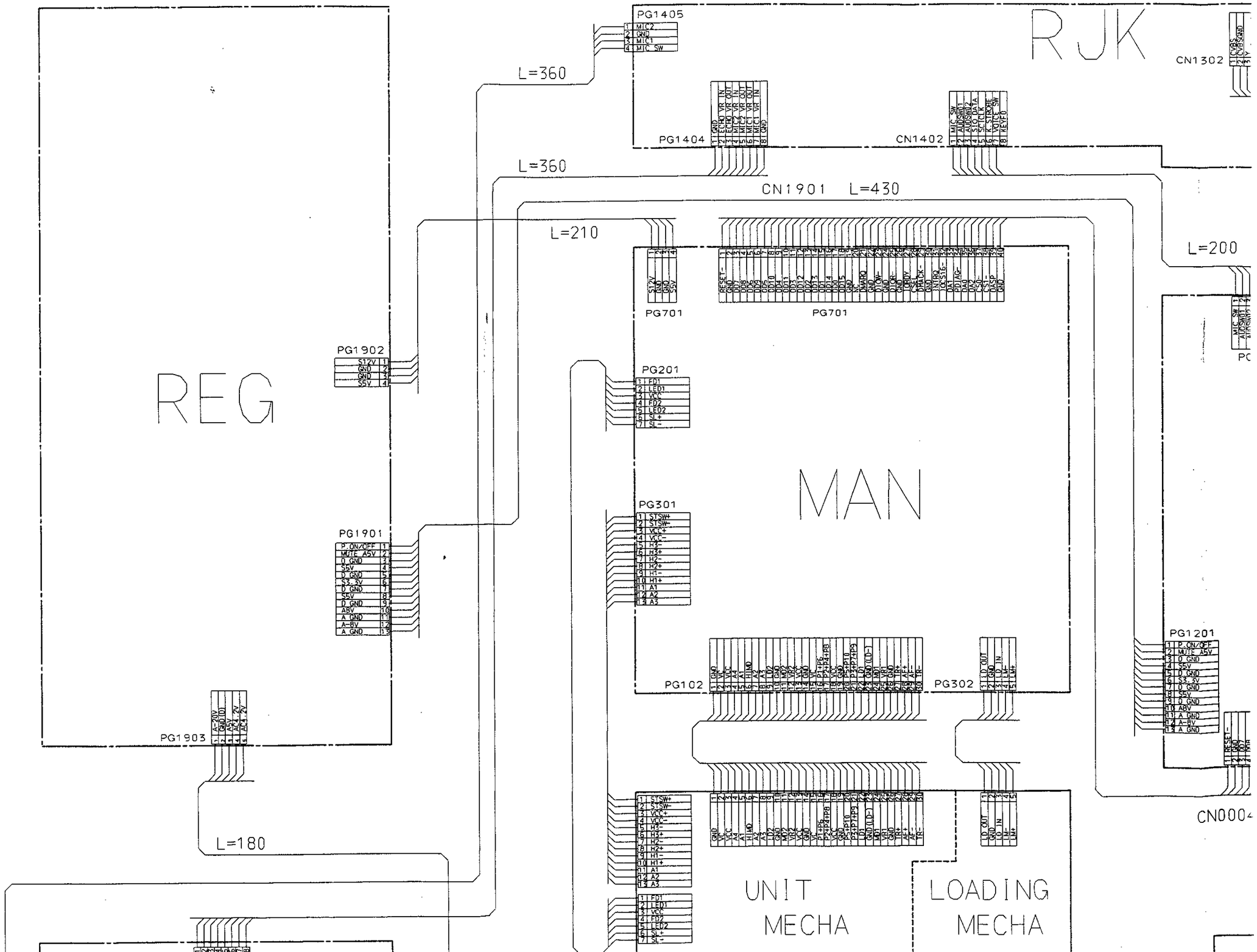
DEC基板
AVデコーダ部
ビデオエンコーダ部 へ

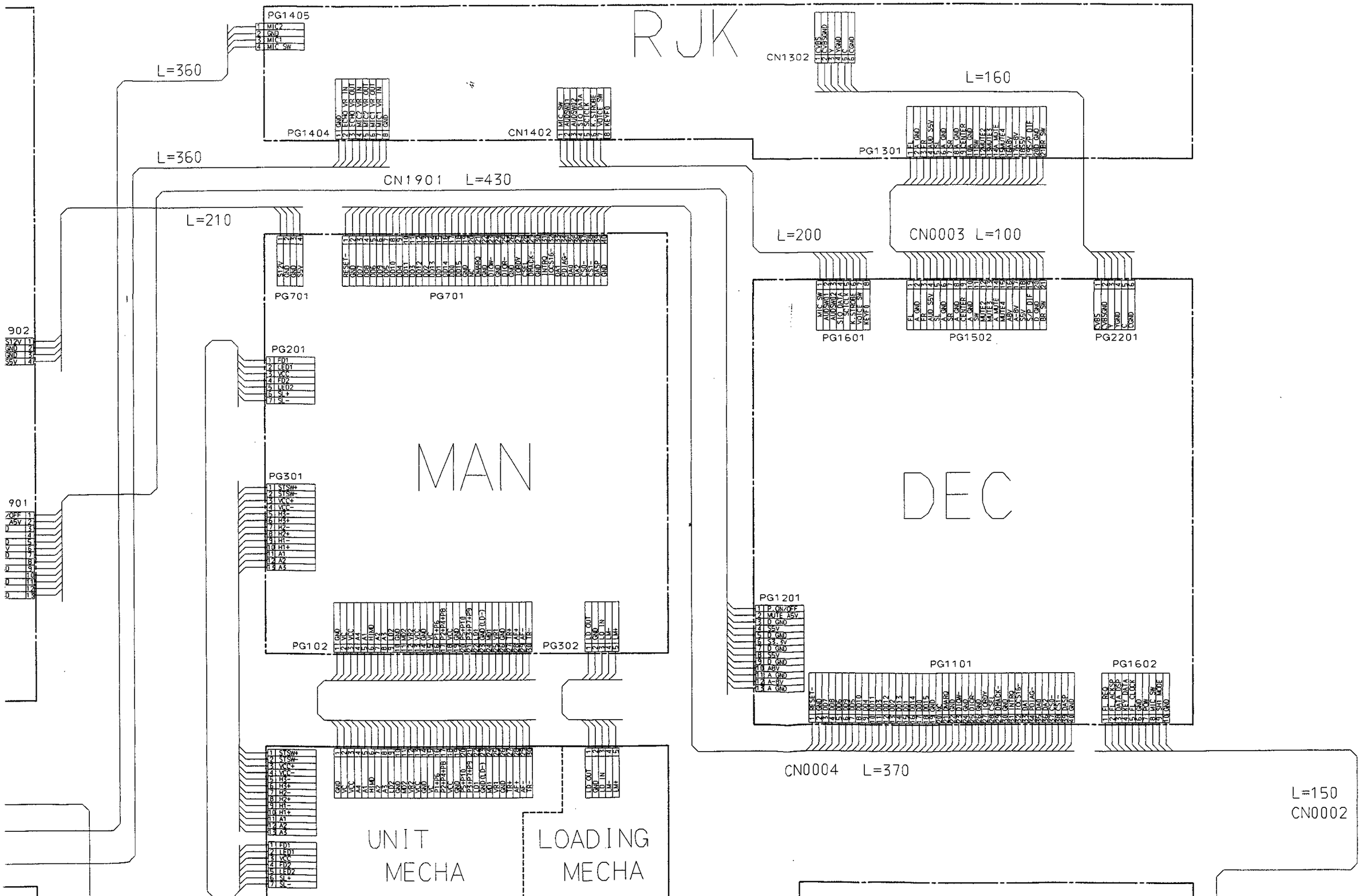
DEC基板
SHマイコン部へ

2 3 4 5

B C D E

9. コネクタ結線図


REG
MAN
RJK
UNIT
MECHA
LOADING
MECHA
PG1405
PG1404
PG1902
PG1901
PG1903
PG701
PG201
PG301
PG102
PG302
PG1201
CN1302
CN1402
CN1901
CN0004
L=360
L=360
L=210
L=430
L=200
L=180


RJK
MAN
DEC
UNIT
MECHA
LOADING
MECHA
PG1405
MIC2
GND
MIC1
MIC_SW
L=360
PG1404
ECHO VR IN
ECHO VR OUT
MIC2 VR IN
MIC2 VR OUT
MIC1 VR IN
MIC1 VR OUT
GND
CN1402
MIC SW
AUDSW01
AUDSW02
SIO DATA
SCTCLK
K STROBE
VOICE SW
KEY0
CN1302
CVBS
CVBSGND
Y
YGND
CGND
CGND
L=160
PG1301
L=360
CN1901 L=430
L=210
PG701
RESET-
GND
D07
D08
D06
D05
D010
D04
D011
D03
D012
D02
D013
D01
D014
D00
D015
GND
NC
DMARQ
DIOW-
GND
DIOR-
GND
IORDY
DMACK-
GND
INTRQ
IOCS16-
DA1
DA0
DA2
CS1-
CS3-
DASP
GND
PG701
S12V
GND
GND
S5V
L=200
CN0003 L=100
PG1601
MIC_SW
AUDSW01
AUDSW02
SIO_DATA
SCTCLK
K_STROBE
VOICE_SW
KEY0
PG1502
FL
FL GND
FR
AUD_S5V
SL
A_GND
SR
GND
CENTER
A_GND
SW
MUTE3
MUTE4
A_MUTE
A8V
A-8V
S5V
S_D_DIF
D_GND
B8_SW
PG2201
CVBS
CVBSGND
Y
YGND
CGND
902
S12V
GND
GND
S5V
PG201
FD1
LED1
VCC+
FD3
LED2
SL+
SL-
901
OFF
A5V
PG301
STSW+
STSW-
VCC+
VCC-
H3+
H3-
H2-
H2+
H1-
H1+
A1
A2
A3
PG102
PG302
LD_OUT
GND
LO_IN
LM-
LM+
PG1201
P_ON/OFF
MUTE_A5V
D_GND
S5V
D_GND
S3.3V
D_GND
S5V
D_GND
A8V
A_GND
A-8V
A_GND
PG1101
PG1602
FL_RCO
FL_ACKSP
FL_DATA
FL_CLOCK
GND
POW
MIC_SW
SHT_MODE
GND
CN0004 L=370
L=150
CN0002

REG

PG1902
S12V 1
GND 2
GND 3
S5V 4

PG1901
P.ON/OFF 1
MUTE A5V 2
D GND 3
S5V 4
D GND 5
S3.3V 6
D GND 7
S5V 8
D GND 9
A8V 10
A GND 11
A-8V 12
A GND 13

PG1903
A-20V 1
GND(D) 2
A5V 3
AC1.2V 4
AC1.2V 5

L=180

MAN

PG201
1 FD1
2 LED1
3 VCC
4 FD2
5 LED2
6 SL+
7 SL-

PG301
1 STSW+
2 STSW-
3 VCC+
4 VCC-
5 H3-
6 H3+
7 H2-
8 H2+
9 H1-
10 H1+
11 A1
12 A2
13 A3

PG102

PG302

PG1201
1 P.ON/OFF
2 MUTE A5V
3 D GND
4 S5V
5 D GND
6 S3.3V
7 D GND
8 S5V
9 D GND
10 A8V
11 A GND
12 A-8V
13 A GND

CN0004

UNIT MECHA

LOADING MECHA

CN1765
GND 1
LCHO VR 2
RCHO VR 3
MIC2 VR 4
MIC2 VR 5
D/C1 VR 6
D/C1 VR 7
GND 8

MVR

CN1702
A-20V 1
GND(D) 2
A5V 3
AC1.2V 4
AC1.2V 5

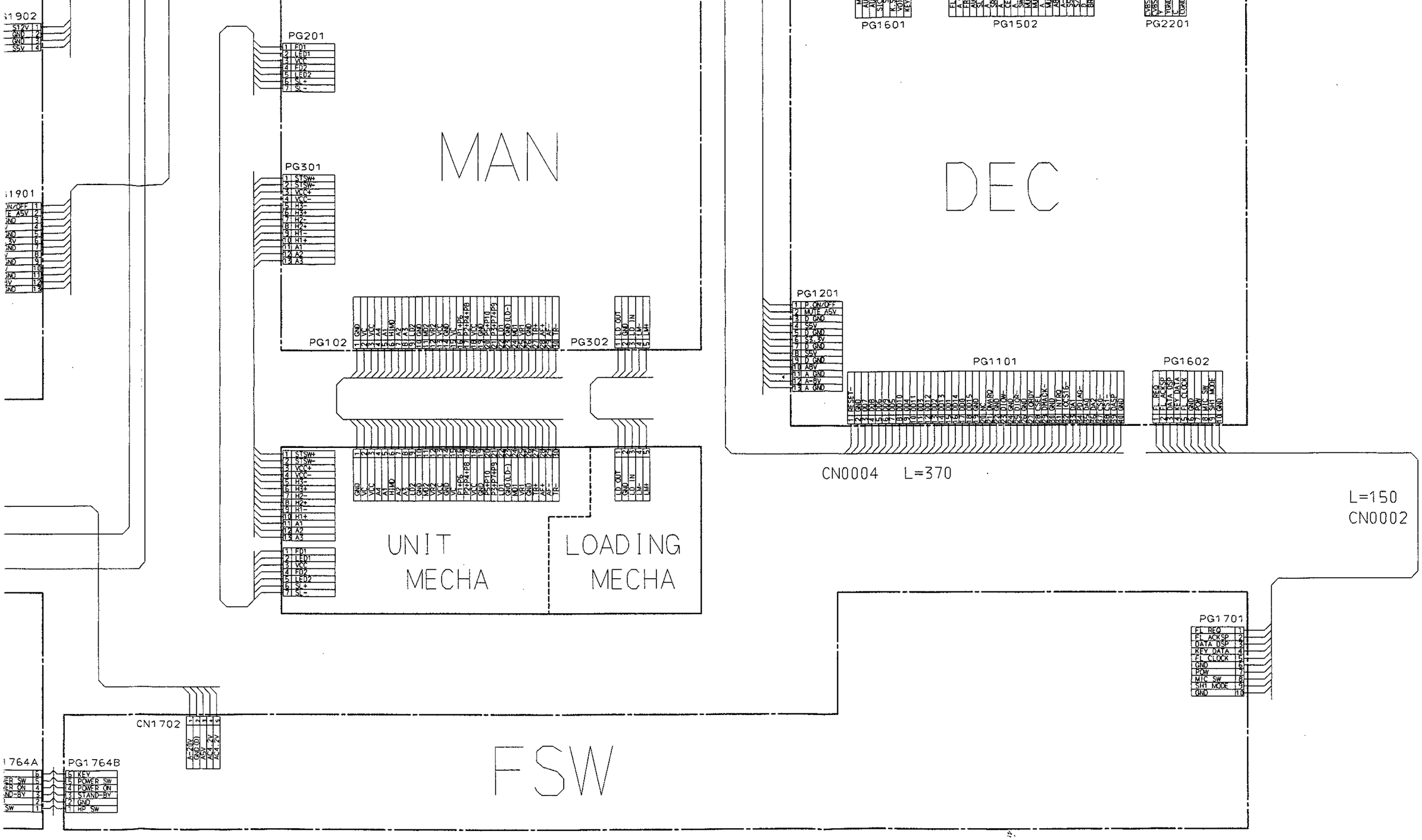
PG1764A
KEY 6
POWER SW 5
POWER ON 4
STAND-BY 3
GND 2
HP SW 1

PG1764B
6 KEY
5 POWER SW
4 POWER ON
3 STAND-BY
2 GND
1 HP SW

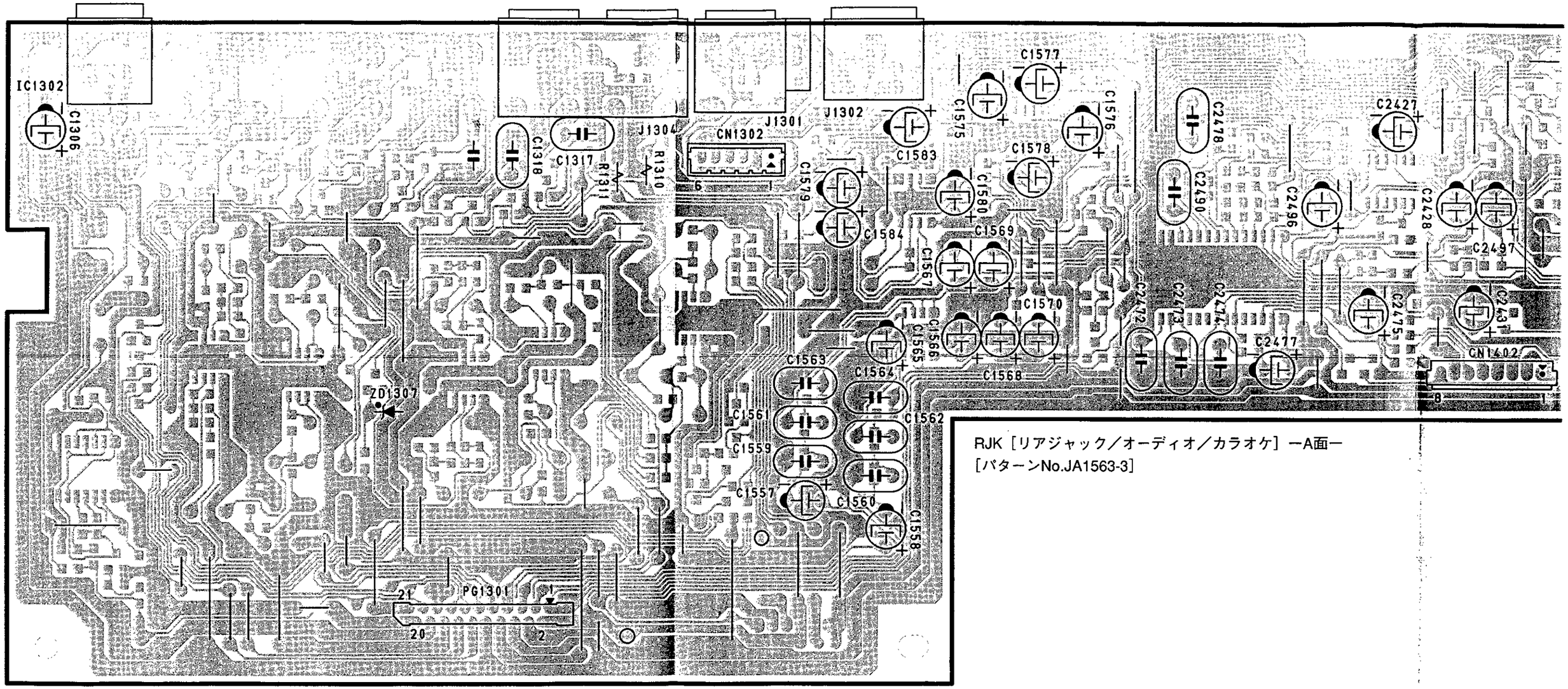
FSW

CN1763
1 MIC2
2 GND
3 MIC1
4 MIC SW

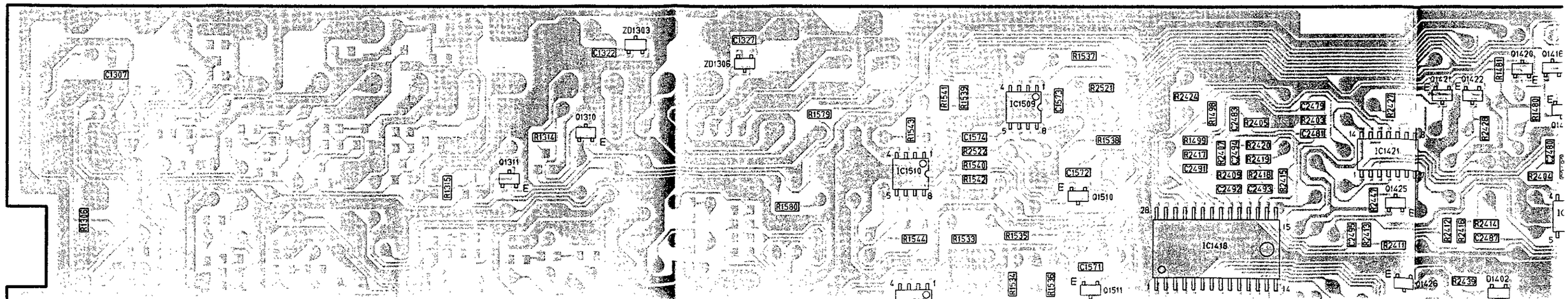
FJK

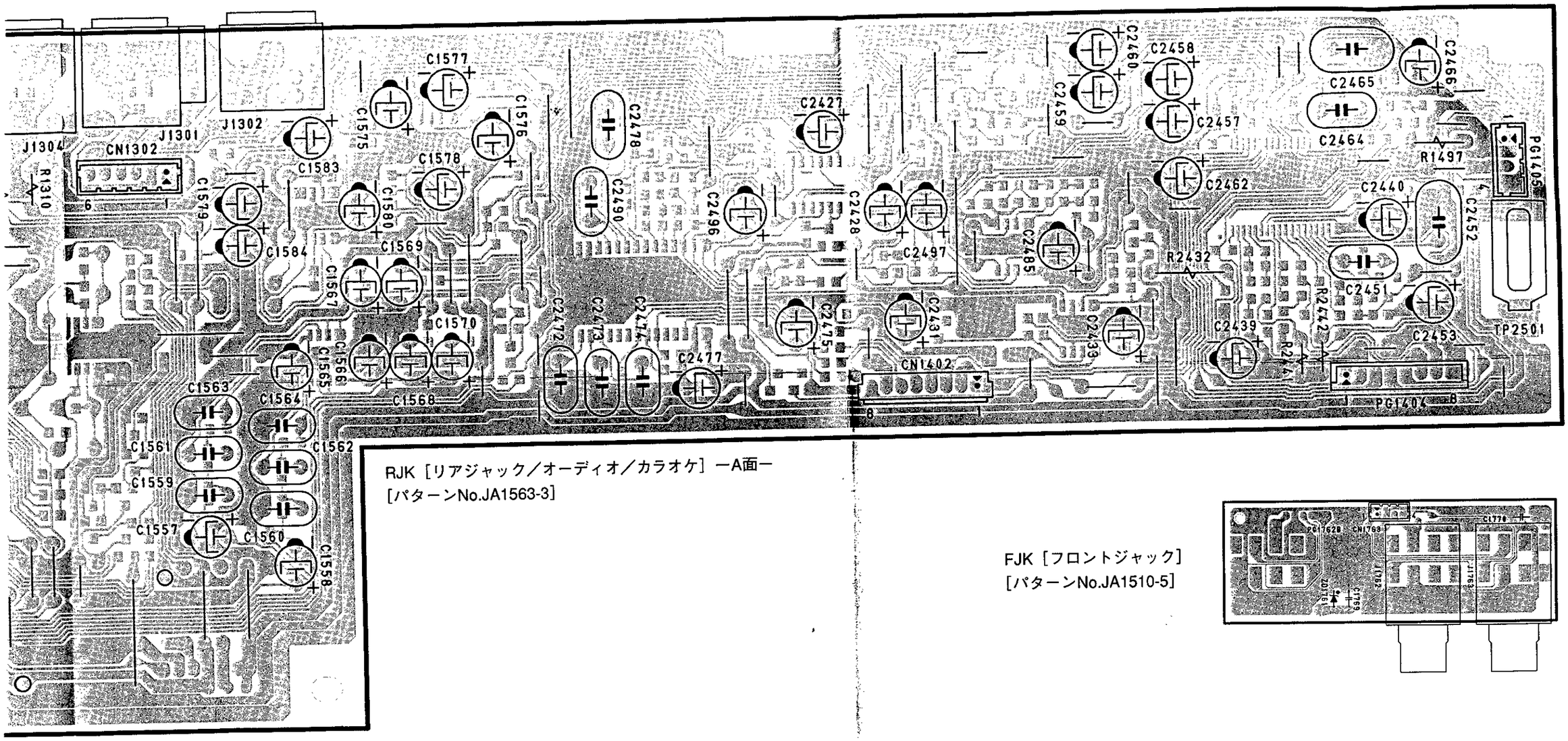

MAN
DEC
UNIT
MECHA
LOADING
MECHA
FSW
PG201
PG301
PG102
PG302
PG1601
PG1502
PG2201
PG1201
PG1101
PG1602
PG1701
PG1902
PG1901
PG1764A
PG1764B
CN1702
CN0004 L=370
L=150
CN0002

10. 基板図



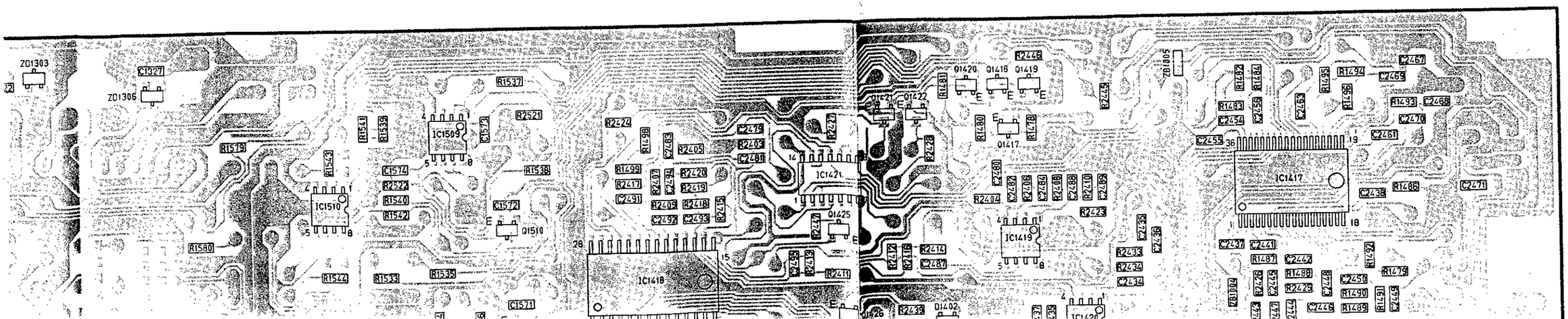
RJK［リアジャック／オーディオ／カラオケ］ーA面ー
［パターンNo.JA1563-3］

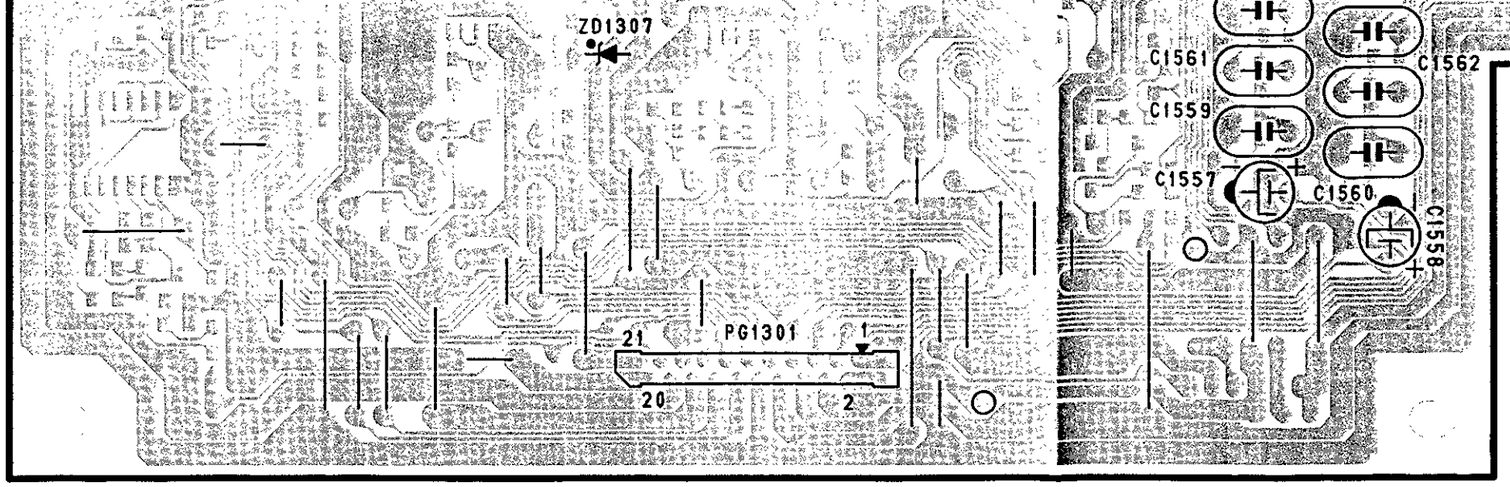




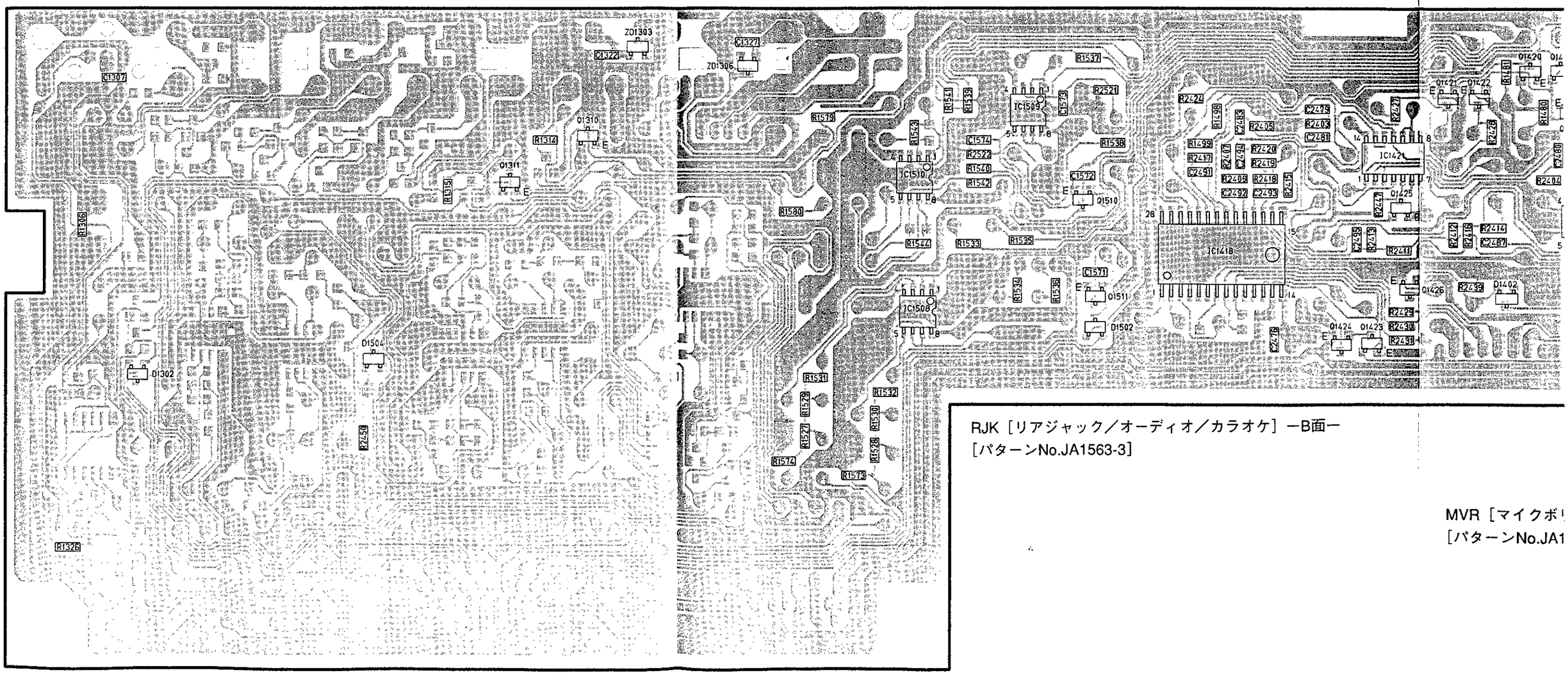
RJK［リアジャック／オーディオ／カラオケ］ーA面ー
［パターンNo.JA1563-3］

FJK［フロントジャック］
［パターンNo.JA1510-5］



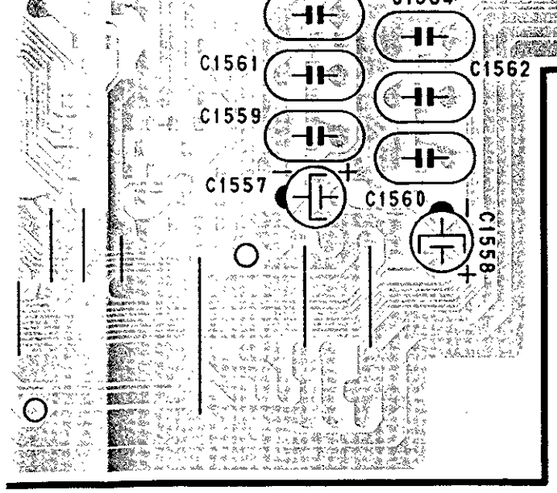


RJK［リアジャック／オーディオ／カラオケ］ーA面ー
［パターンNo.JA1563-3］

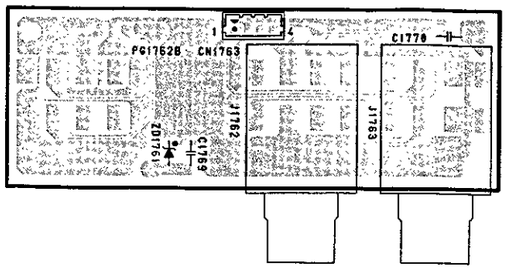


RJK［リアジャック／オーディオ／カラオケ］ーB面ー
［パターンNo.JA1563-3］

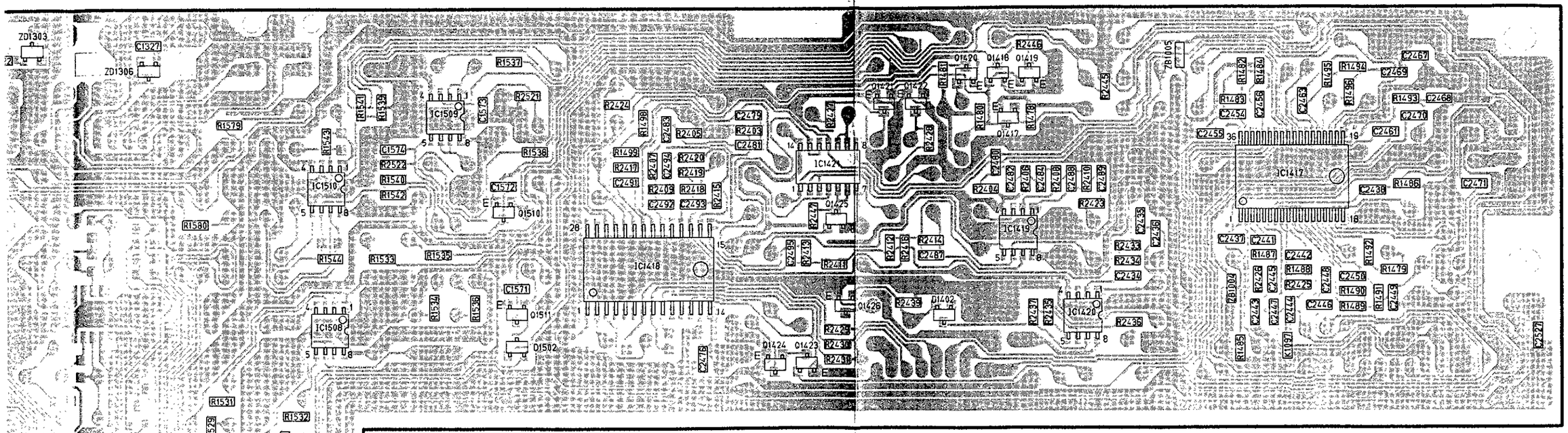
MVR［マイクボ
［パターンNo.JA1



RJK［リアジャック／オーディオ／カラオケ］ーA面ー
［パターンNo.JA1563-3］



FJK［フロントジャック］
［パターンNo.JA1510-5］



RJK［リアジャック／オーディオ／カラオケ］ーB面ー
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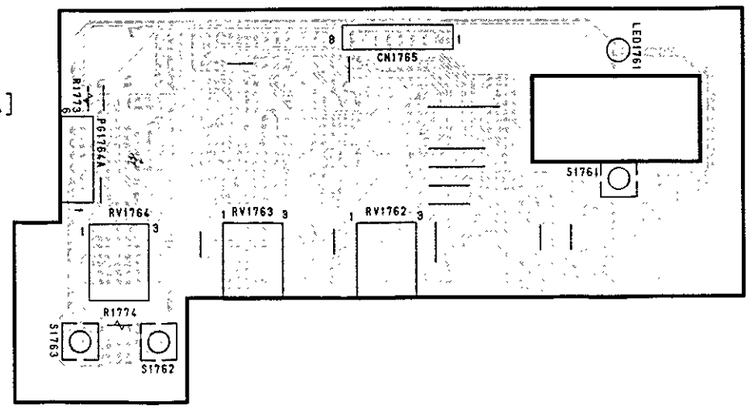

MVR［マイクボリューム］
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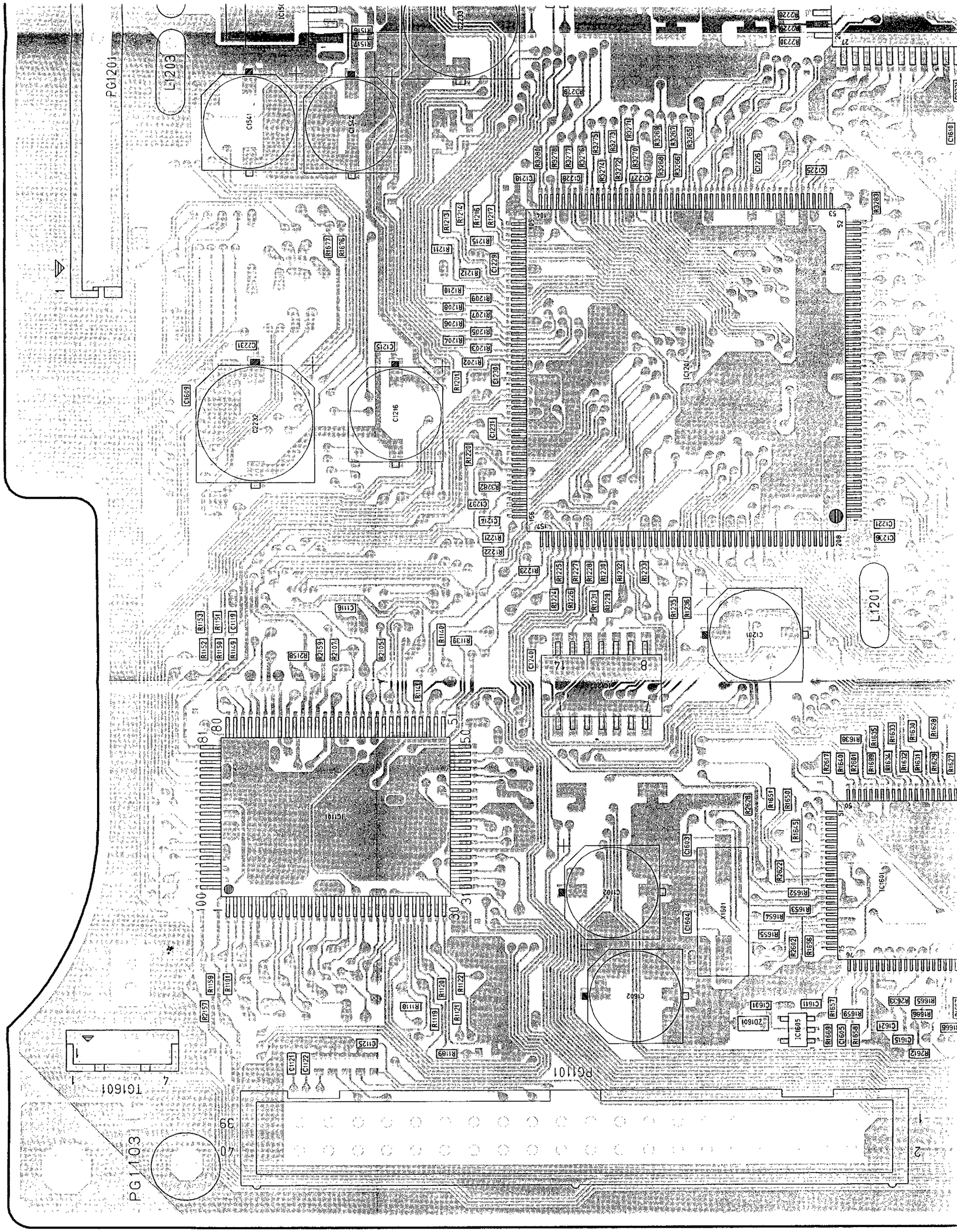
PG1201
L1203
C1541
C1522
C1233
R1510
R1509
R2230
R2228
R3278
R3280
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TG1601
PG1103
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C1611
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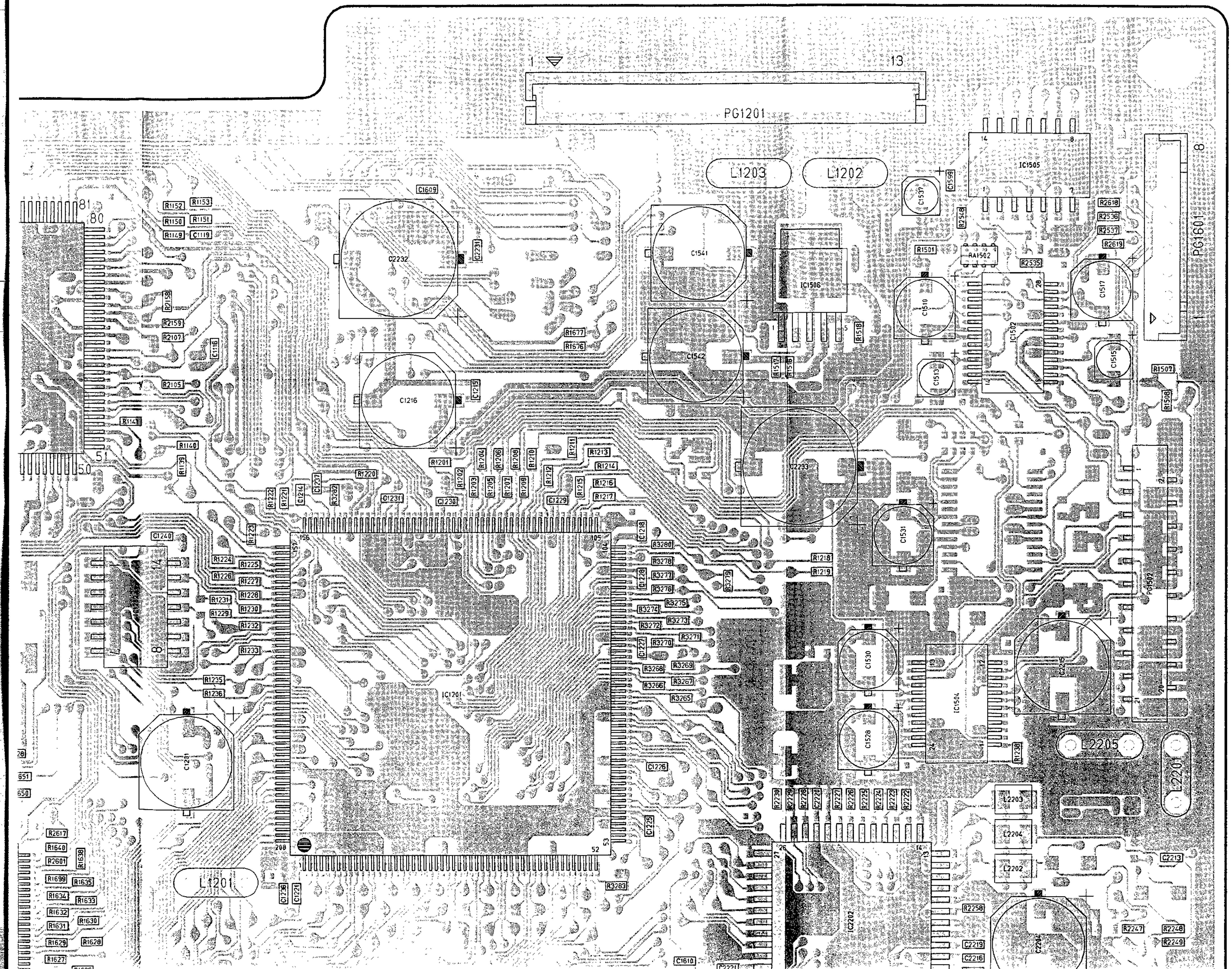
R1668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C1530
C1528
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IC2202
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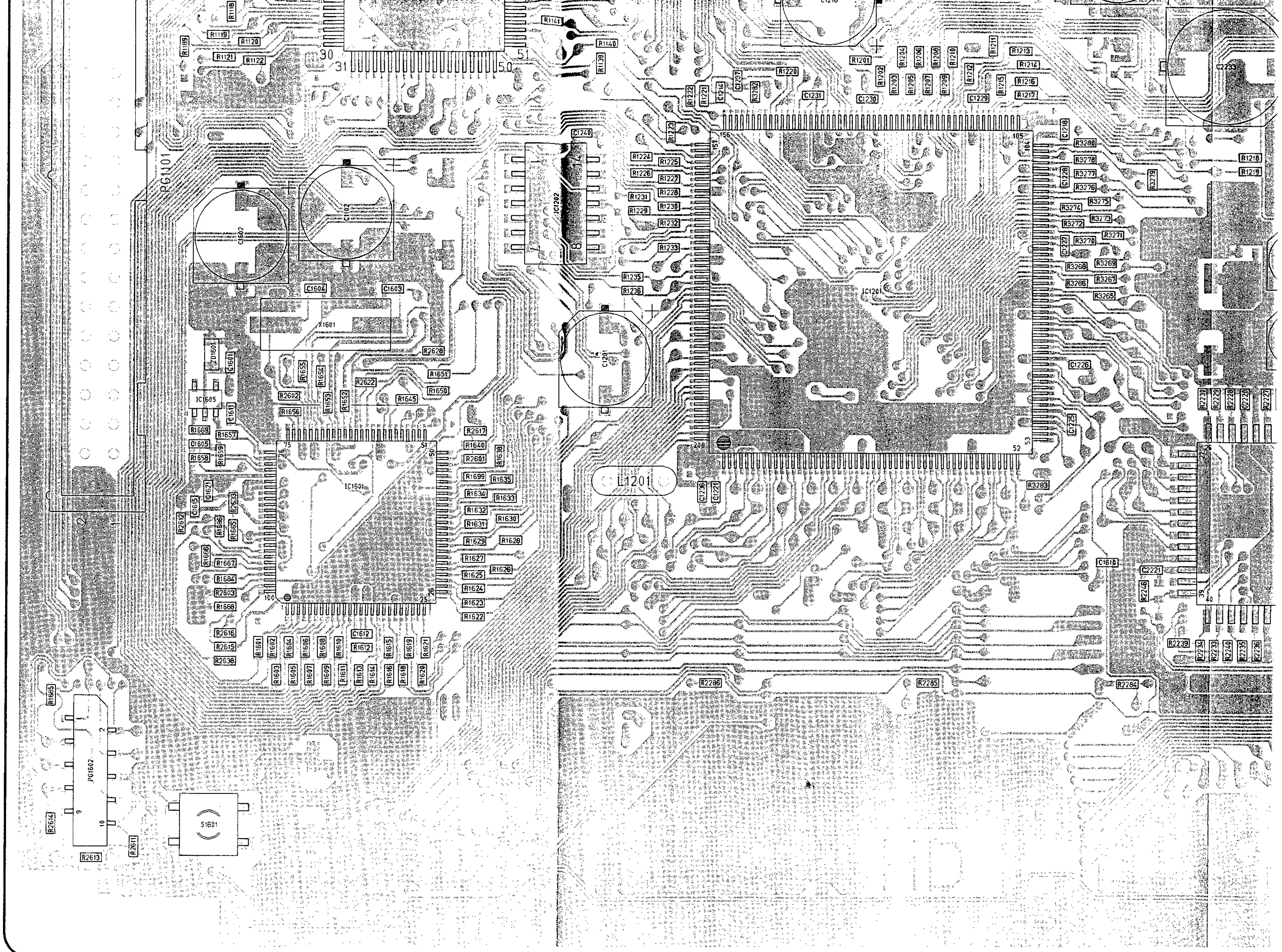
L2202
PG1502



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S1601
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R1122
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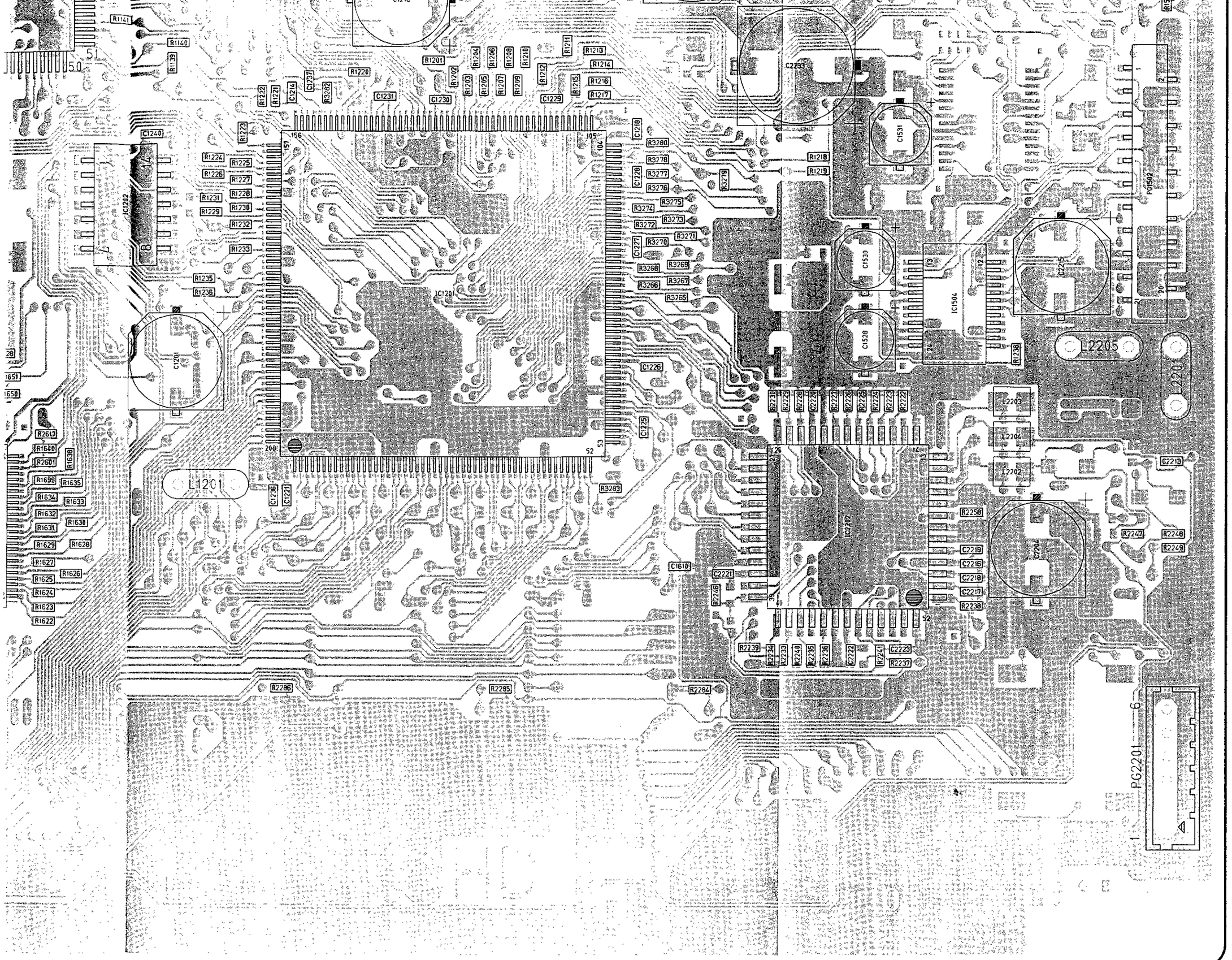
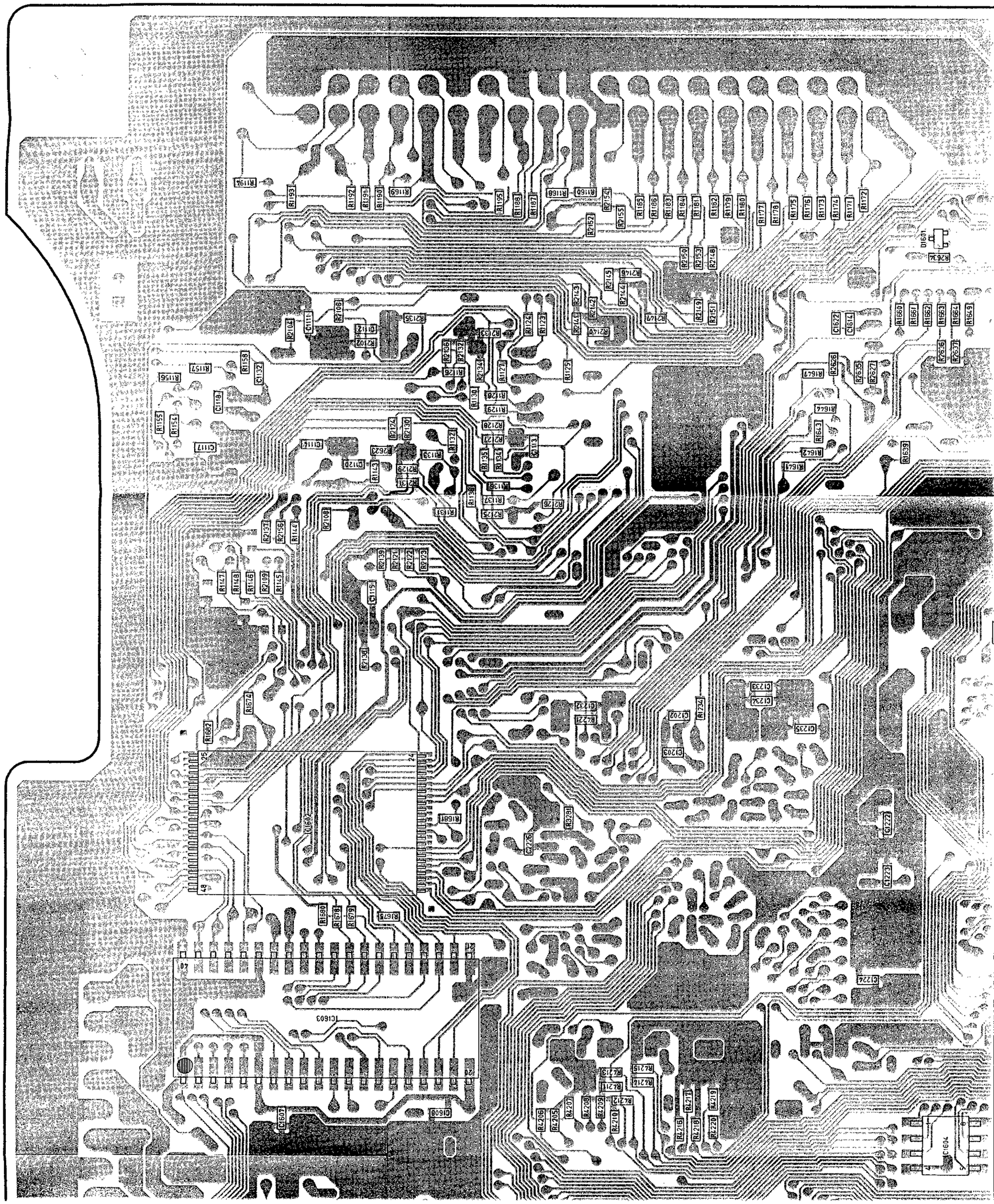


DEC［メイン］ーA面ー
［パターンNo.JA1507-5］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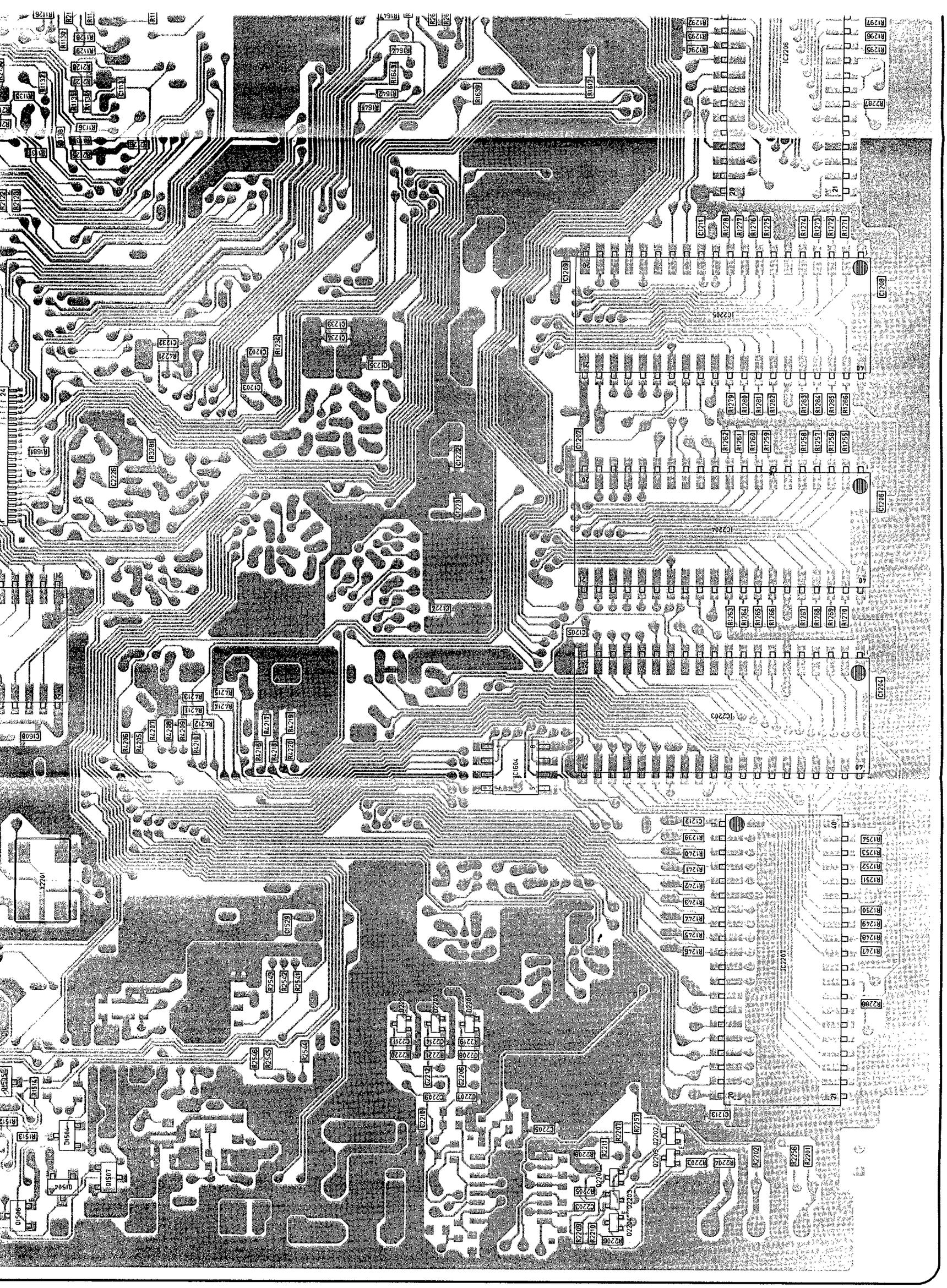
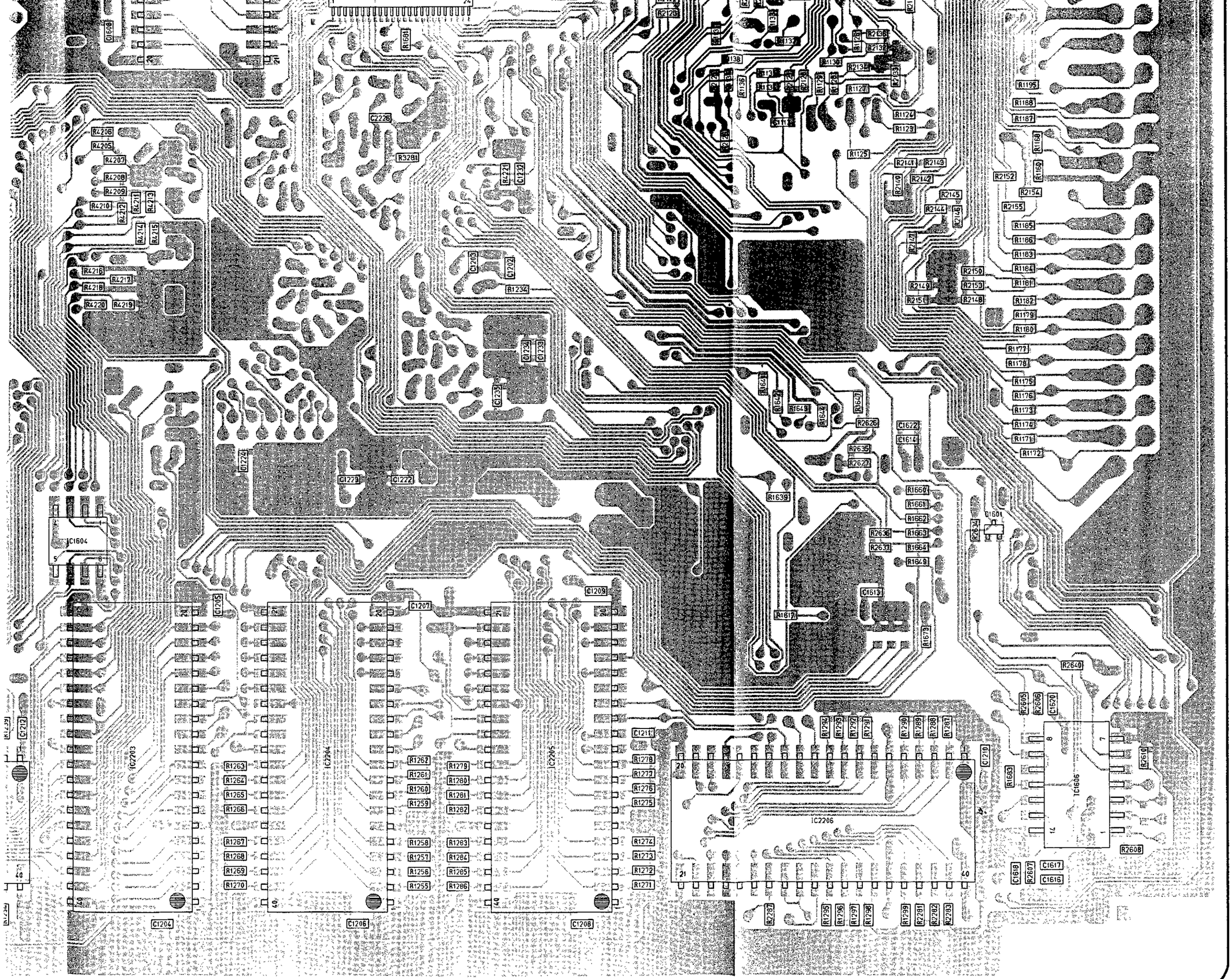
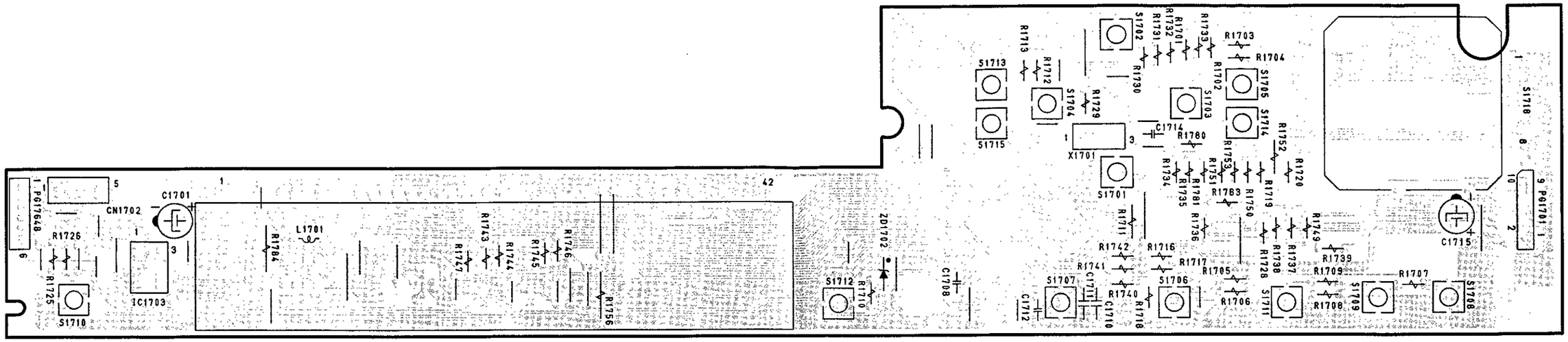
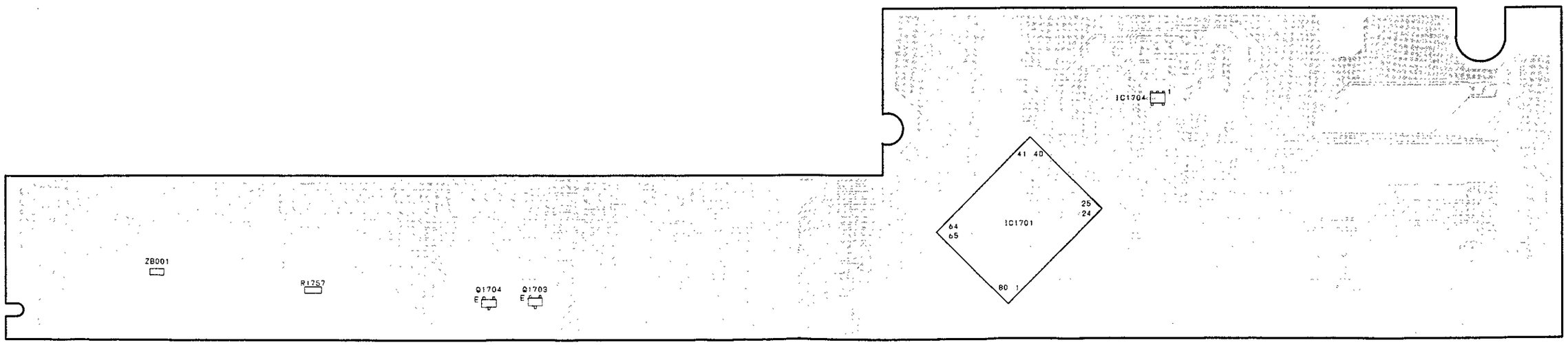




DEC［メイン］ーB面ー
［パターンNo.JA1507-5］

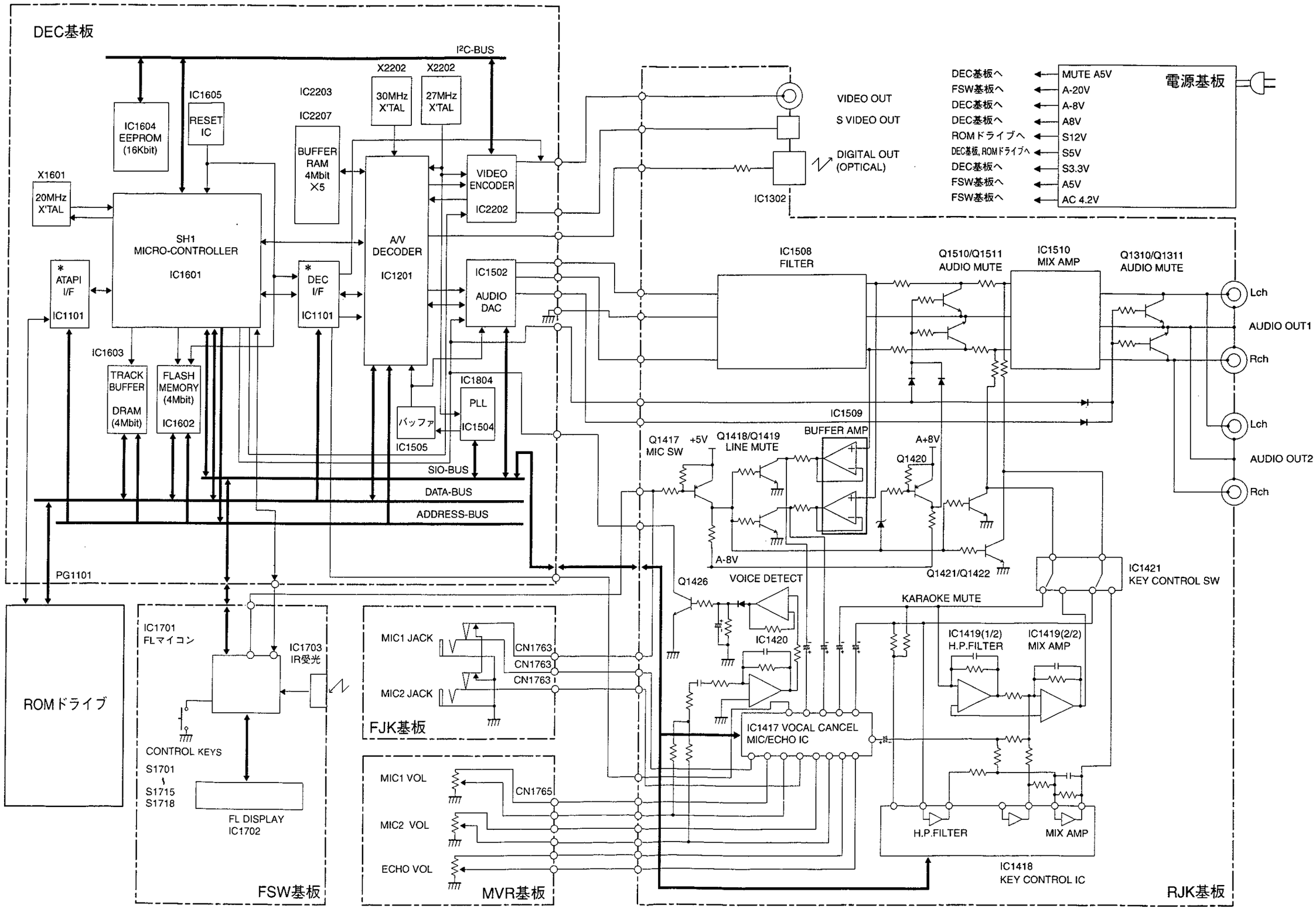


FSW［フロントスイッチ／FL管］ーA面ー
［パターンNo.JA1563-3］

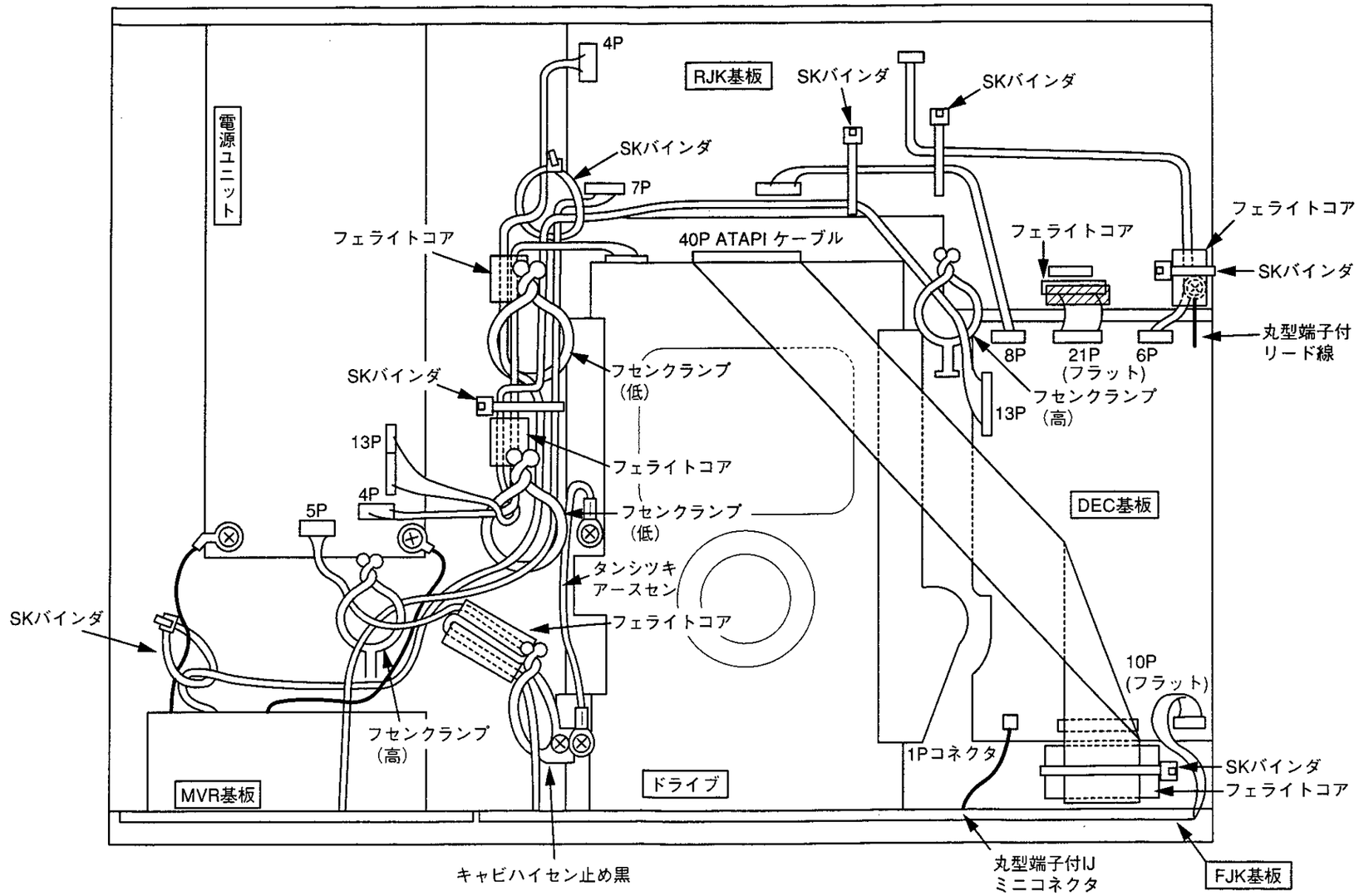


FSW［フロントスイッチ／FL管］ーB面ー
［パターンNo.JA1563-3］

11. ブロック図


DEC基板
I²C-BUS
X2202
X2202
IC1605
IC2203
IC2207
30MHz X'TAL
27MHz X'TAL
IC1604 EEPROM (16Kbit)
RESET IC
BUFFER RAM 4Mbit ×5
X1601
20MHz X'TAL
VIDEO ENCODER IC2202
SH1 MICRO-CONTROLLER IC1601
A/V DECODER IC1201
IC1502 AUDIO DAC
* ATAPI I/F IC1101
* DEC I/F IC1101
IC1603
TRACK BUFFER DRAM (4Mbit)
FLASH MEMORY (4Mbit) IC1602
IC1804
PLL IC1504
バッファ IC1505
SIO-BUS
DATA-BUS
ADDRESS-BUS
PG1101
VIDEO OUT
S VIDEO OUT
DIGITAL OUT (OPTICAL)
IC1302
DEC基板へ MUTE A5V
FSW基板へ A-20V
DEC基板へ A-8V
DEC基板へ A8V
ROMドライブへ S12V
DEC基板, ROMドライブへ S5V
DEC基板へ S3.3V
FSW基板へ A5V
FSW基板へ AC 4.2V
電源基板
IC1508 FILTER
Q1510/Q1511 AUDIO MUTE
IC1510 MIX AMP
Q1310/Q1311 AUDIO MUTE
Lch
AUDIO OUT1
Rch
Lch
AUDIO OUT2
Rch
IC1509
BUFFER AMP
Q1417 MIC SW
+5V
Q1418/Q1419 LINE MUTE
A+8V
Q1420
A-8V
Q1421/Q1422
IC1421 KEY CONTROL SW
Q1426
VOICE DETECT
IC1420
KARAOKE MUTE
IC1419(1/2) H.P.FILTER
IC1419(2/2) MIX AMP
IC1417 VOCAL CANCEL MIC/ECHO IC
H.P.FILTER
MIX AMP
IC1418 KEY CONTROL IC
RJK基板
ROMドライブ
IC1701 FLマイコン
IC1703 IR受光
CONTROL KEYS
S1701
S1715
S1718
FL DISPLAY IC1702
FSW基板
MIC1 JACK
MIC2 JACK
CN1763
CN1763
CN1763
FJK基板
MIC1 VOL
MIC2 VOL
ECHO VOL
CN1765
MVR基板

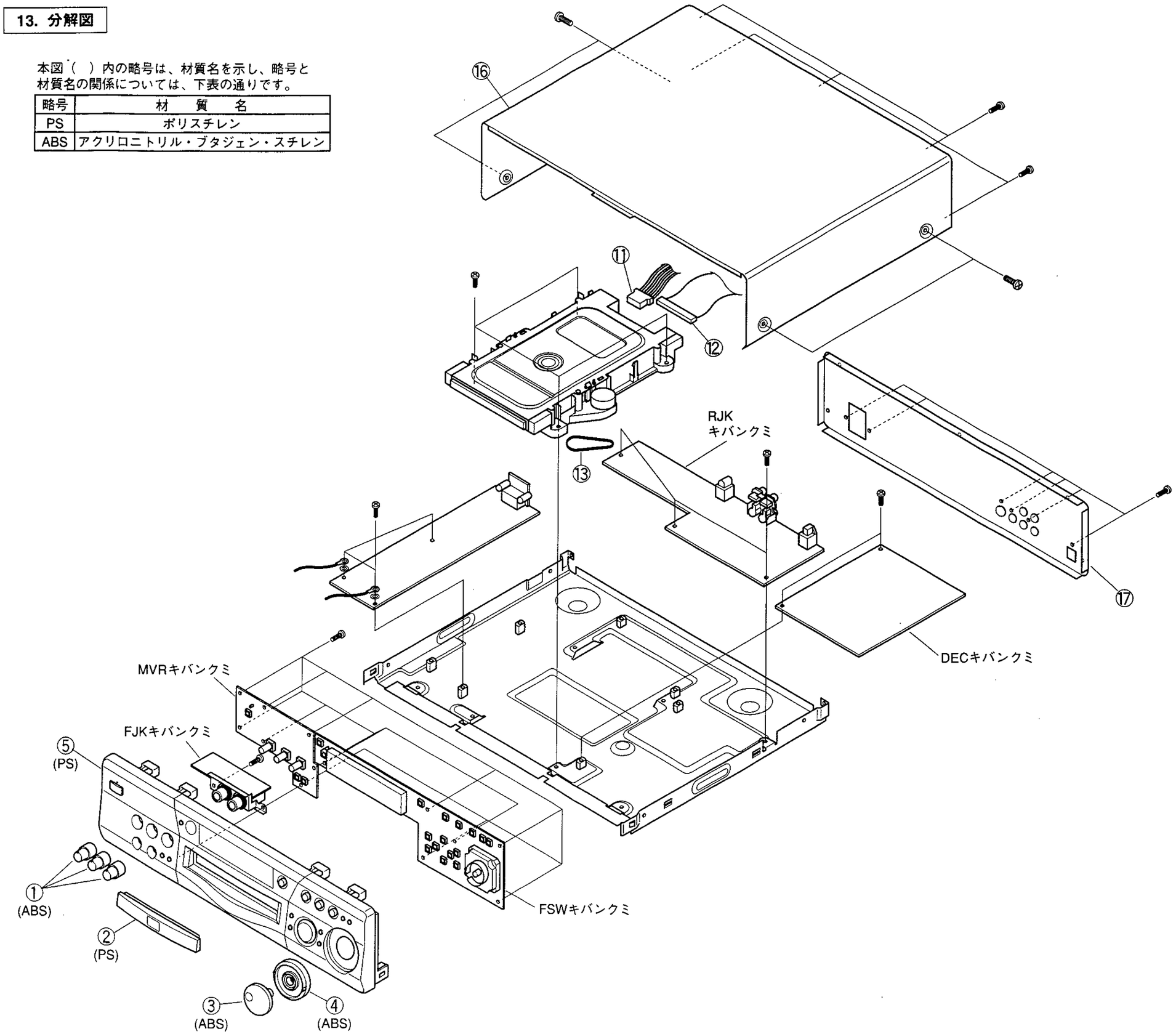
12. 布線図


4P
RJK基板
SKバインダ
SKバインダ
電源ユニット
SKバインダ
7P
フェライトコア
40P ATAPI ケーブル
フェライトコア
フェライトコア
SKバインダ
丸型端子付
リード線
8P
21P
(フラット)
6P
フセンクランプ
(低)
SKバインダ
フセンクランプ
(高)
13P
13P
フェライトコア
4P
5P
フセンクランプ
(低)
DEC基板
タンシツキ
アースセン
SKバインダ
フェライトコア
10P
(フラット)
1Pコネクタ
SKバインダ
フェライトコア
フセンクランプ
(高)
MVR基板
ドライブ
キャビハイセン止め黒
丸型端子付IJ
ミニコネクタ
FJK基板

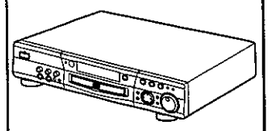
13. 分解図

本図（ ）内の略号は、材質名を示し、略号と材質名の関係については、下表の通りです。

略号	材　質　名
PS	ポリスチレン
ABS	アクリロニトリル・ブタジェン・スチレン



14. PARTS LIST



Reserve item	338-04	Sale start day	July 1998
Model	DV-K2		
Product name	DVD player	Service guide No.	B002

1. ※ mark is put for newly adopted part. Prices are those of July 1998.
2. ⚠ mark is put for a designated part by safety consideration.

Distinctive marks	Circuit No.	Part name (specification and usage)	Part No.		Packing unit	T	¥	Remarks
※	1	Knob	DV-K2	002	1	210	300	
※	2	Panel tray set	DV-K2	003	1	560	800	
※	3	Knob (JOG)	DV-K2	004	1	210	300	
※	4	Knob (SHU)	DV-K2	005	1	210	300	
※	5	Panel front set	DV-K2	006	1	2100	3000	
※	11	Connector (4PIN)	DV-K2	009	1	210	300	
※	12	Connector (40PIN)	DV-K2	010	1	350	500	
※	13	Rubber belt Cover top	DV-K2	011	1	210	300	
※	16	Panel rear set	DV-K2	012	1	1260	1800	
※	17		DV-K2	013	1	700	1000	
※	801	Cord (3PIN)	DV-K2	014	1	700	1000	
※	802	Remote control (DV-RM2)	DV-K2	001	1	1050	1500	
※⚠	803	Cord AC	DV-K2	015	1	700	1000	

The prices listed above are not including the value added taxes.

OPTICAL STORAGE DEPARTMENT, IMAGE INFORMATION
MEDIA DIVISION, HITACHI LTD.

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